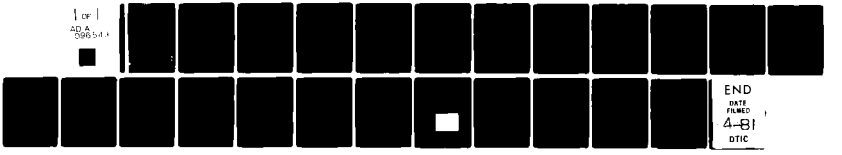
AD-A096 543 ELECTRONICS RESEARCH LAB ADELAIDE (AUSTRALIA) F/G 20/5
A FAST, HIGH VOLTAGE, AVALANCHE TRANSISTOR Q SWITCH DRIVER.(U)
AUG 80 B A SEE

UNCLASSIFIED ERL-0154-TM NL

1 OF 1
AD A 096543



END
DATE FILMED
4-81
DTIC

ERL-0154-TM

AR-002-028

DEPARTMENT OF DEFENCE

DEFENCE SCIENCE AND TECHNOLOGY ORGANISATION

ELECTRONICS RESEARCH LABORATORY

DEFENCE RESEARCH CENTRE SALISBURY
SOUTH AUSTRALIA

TECHNICAL MEMORANDUM

ERL-0154-TM

A FAST, HIGH VOLTAGE, AVALANCHE TRANSISTOR Q SWITCH DRIVER

B.A. SEE

COPY No. 15

AUGUST 1980

AR-002-028

DEPARTMENT OF DEFENCE

DEFENCE SCIENCE AND TECHNOLOGY ORGANISATION

ELECTRONICS RESEARCH LABORATORY

(1) TECHNICAL MEMORANDUM

(14) ERL-0154-TM

(6) A FAST, HIGH VOLTAGE, AVALANCHE TRANSISTOR Q SWITCH DRIVER.

(10) B.A./See

SUMMARY

(12) 24

This paper describes the development of a fast high voltage switching circuit using avalanche transistors.

The circuit was found eminently suitable for Electro-Optic Q Switching and cavity dumping of lasers.

Many transistor types have been used to drive Q switch elements but in most cases the avalanche chain must be carefully matched to the load.

The circuit described here used the transistor type 2N5192 which was found to have a wide operating range thus allowing the chain to be easily matched to the Q switch voltage requirements. In addition it has proven very robust and not easily damaged by over voltage.

Approved for Public Release

(11) Aug 80

POSTAL ADDRESS: Chief Superintendent, Electronics Research Laboratory, Box 2151, GPO, Adelaide, South Australia, 5001.

DOCUMENT CONTROL DATA SHEET

Security classification of this page: UNCLASSIFIED

1 DOCUMENT NUMBERS		2 SECURITY CLASSIFICATION	
AR Number:	AR-002-028	a. Complete Document:	Unclassified
Report Number:	ERL-0154-TM	b. Title in Isolation:	Unclassified
Other Numbers:		c. Summary in Isolation:	Unclassified

3 TITLE: A FAST, HIGH VOLTAGE, AVALANCHE TRANSISTOR Q SWITCH DRIVER

4 PERSONAL AUTHOR(S):

B.A. See

5 DOCUMENT DATE: August 1980

6 6.1 TOTAL NUMBER OF PAGES: 17

6.2 NUMBER OF REFERENCES: 13

7 7.1 CORPORATE AUTHOR(S):

Electronics Research Laboratory

7.2 DOCUMENT SERIES AND NUMBER

Electronics Research Laboratory 0154-TM

8 REFERENCE NUMBERS

a. Task: 79/049

b. Sponsoring Agency: DEFENCE

9 COST CODE: 217599

10 IMPRINT (Publishing organisation)

Defence Research Centre Salisbury

11 COMPUTER PROGRAM(S) (Title(s) and language(s))

12 RELEASE LIMITATIONS (of the document):

Approved for Public Release

12.0	OVERSEAS	NO		P.R.	1	A		B		C		D		E	

Security classification of this page: UNCLASSIFIED

Security classification of this page: UNCLASSIFIED

13 ANNOUNCEMENT LIMITATIONS (of the information on these pages):

No limitation

14 DESCRIPTORS:		15 COSATI CODES
a. EJC Thesaurus Terms	Avalanche effect (electronics) Lasers Transistors Switching circuits Electrooptics Q switched lasers	2005
b. Non-Thesaurus Terms	Avalanche transistors Cavity dumping WRELADS 2N5192 transistors	

16 LIBRARY LOCATION CODES (for libraries listed in the distribution):

17 SUMMARY OR ABSTRACT:
(if this is security classified, the announcement of this report will be similarly classified)

This paper describes the development of a fast high voltage switching circuit using avalanche transistors.

The circuit was found eminently suitable for Electro-Optic Q Switching and cavity dumping of lasers.

Many transistor types have been used to drive Q switch elements but in most cases the avalanche chain must be carefully matched to the load.

The circuit described here used the transistor type 2N5192 which was found to have a wide operating range thus allowing the chain to be easily matched to the Q switch voltage requirements. In addition it has proven very robust and not easily damaged by over voltage.

Security classification of this page: UNCLASSIFIED

TABLE OF CONTENTS

		Page No.
1.	INTRODUCTION	1
2.	THE SELECTION OF A TRANSISTOR	1
3.	THE AVALANCHE CHAIN	3
	3.1 Voltage rise time	3
	3.2 Optical switching speed	6
4.	ALTERNATIVE CIRCUIT FORMS	7
	4.1 Q switch circuit	7
	4.2 Cavity dump drive circuit	7
	4.3 Pulse gating	7
5.	CONCLUSION	8
	REFERENCES	9

LIST OF TABLES

1.	AN ASSESSMENT OF TRANSISTORS IN THE AVALANCHE MODE	2
2.	THE EFFECT OF A CAPACITIVE LOAD ON A SINGLE TRANSISTOR	4
3.	THE EFFECT OF A CAPACITIVE LOAD ON A 6 TRANSISTOR CHAIN	5
4.	THE EFFECT OF A CAPACITIVE LOAD ON A TIGHTLY PACKED CHAIN	6

LIST OF FIGURES

1. Test circuits for Avalanche transistors
2. 2N2222 Avalanche characteristics
3. 2N5192 Avalanche characteristics
4. Avalanche transistor chain
5. Equivalent circuit in ON state
6. Voltage step for 6 transistor chain
7. Circuit for pulse output
8. PTM Q switch drive circuit

1. INTRODUCTION

The WRELADS laser system being developed in the Electronics Research Laboratory requires a high repetition rate laser delivering pulses of 5 ns FWHM. As part of a study on lasers to meet this requirement, the Pulse Transmission Mode (PTM) laser was examined. In this mode, the laser cavity is closed with 100% reflecting mirrors at both ends. The laser is electro-optically Q switched in the normal manner then when the energy density in the cavity reaches its peak, the Q switch is shut very quickly. The energy drains from the cavity via the polarising prism in the time it takes to make one round trip of the cavity. Short pulses can therefore be produced fairly easily. To operate the Q switch in this manner requires two high voltage switching operations in which the first need only be short compared to the pulse evolution time (of the order of 50 ns) whilst the second needs to be considerably faster, ideally less than the time for one round trip of the cavity (2d/c , where d is the cavity length).

Hook et al(ref.1,2) investigated this method of operation using gas filled Krytron tubes for the switching. The circuit reported by them(ref.2) was used here but our version was found to be unreliable in operation.The results obtained by Hook et al were for a fairly long Q switched pulse (60 ns). Triggering in the circuit was performed optically with a high voltage vacuum photodiode sensing the leading edge of the Q switch pulse. For a symmetric Q switched pulse , approximately 30 ns are available in which to achieve switching at the peak of the pulse. If the Q switch pulse is short, say 20 ns , then the Krytron triggering delay of 20 ns is unacceptable as triggering would occur too late. In addition the life of the Krytron was not expected to exceed 10^5 firings.

For these reasons the Krytron was not considered suitable as a switch for our application. However Ley et al(ref.3), had used avalanche transistor chains to provide the fast, high voltage ($\cong$1 kV), trigger pulse to a Krytron. By using more transistors in the chain, it was decided that one could use the avalanche device in place of the Krytron.

2. THE SELECTION OF A TRANSISTOR

A literature survey established that many authors had used transistors in the avalanche mode(ref.4 to 7) but there seemed to be no clear reasons for a particular choice of transistor type. The course followed was to procure those transistors referred to in the literature together with a wide selection of other transistors which were readily available and test them all in suitable test circuits.

Good background information on avalanche switching is available in the Motorola Switching Transistor Handbook, a Ferranti publication titled "The Use of Transistors in the Avalanche Mode" and various articles(ref.8 to 11), most of which were published in the early 1960's.

A simple test circuit, figure 1(a), was built to test each transistor individually. A 5 V pulse was applied at the input to the base and the voltage across the transistor was increased until it began to fire. This voltage was noted as the lower working limit. The voltage was then increased further until the transistor went into a free running avalanche, erratic and untriggered. This was noted as the upper voltage limit.

In Table 1, a list of transistor types tested is shown, together with approximate lifetimes and upper and lower voltage limits. From an examination of the properties of the transistors listed a selection was made and larger quantities of the more promising types were obtained and subjected

to more extensive testing.

TABLE 1. AN ASSESSMENT OF TRANSISTORS IN THE AVALANCHE MODE

Type	Upper voltage range	Lower voltage range	Approximate rise time (ns)
AX6101	142	86	2.0
AX8001	139	92	1.8
BFY50	125	100	1.5
MPS6520	122	84	1.5
SE4010	193	124	1.7
ZTX300	115	79	1.6
TT3642	102	93	1.4
2N697	147	97	1.7
2N910	132	97	1.8
2N1482	212	172	2.0
2N2102	208	202	1.8
2N2218	101	99	1.5
2N2222	116	88	1.7
2N2405	176	125	2.6
2N2484	137	124	1.7
2N2714	133	83	1.5
2N3019	175	140	
2N3055	165	160	
2N3503	199	159	1.5
2N3565	196	112	2.1
2N3568	160	144	1.7
2N3569	179	124	1.6
2N3641	195	183	1.7
2N3643	128	85	1.4
2N3694	130	92	2.5
2N3707	118	103	1.7
2N3904	105	92	4.2
2N3923	334	242	5.0
2N4300	160	132	2.2
2N4400	103	65	1.8
2N4922	262	163	4.0
2N5192	211	142	2.0

One characteristic not measured by the circuit of figure 1(a) is the voltage drop across the transistor in the ON state. To measure this a test circuit as in figure 1(b) is helpful. A pulse forming network is used to give a long pulse (≅200 ns) so that fast transient voltages can subside and allow the ON voltage to be read on an oscilloscope free of interference.

The results of further testing are shown in the histograms of figures 2 and 3 for two transistor types. Figure 2 is for the 2N2222 transistor used by some workers. Note that its characteristics show a fairly wide spread. In addition, if the upper voltage limit were exceeded the transistor was often irreversibly damaged. Figure 3 shows the results for the transistor finally selected, the 2N5192. It has a high operating voltage, a wide operating range and was found to be very robust, ie it is not easily damaged by over voltage. This transistor had previously been used by Mr V.D. Woolley of this group, as a driver for a light emitting diode in the avalanche mode.

Using the circuit of figure 1(b), the ON voltage for the 2N5192 was found to be ≅20 V.

3. THE AVALANCHE CHAIN

The avalanche chain is essentially the same as that used by Ley et al(ref.3) and is shown in figure 4. A small capacitor across the bottom (triggered) transistor was used to increase the reliability of triggering. Note that the accessible switched voltage at the emitter of the top transistor is less than the full supply voltage due to the dividing action of the resistor chain. Resistor R_L may be smaller than the others in the chain but it limits the current in the ON state and cannot be reduced too far or the transistors will latch on causing certain failure. For the 2N5192 the latching current was found from the circuit of figure 1(a) by reducing the resistance gradually until latching occurred. The test can only be done once on a transistor because it damages the device. Although the power dissipation may be less than the rated power when operated in the normal mode, the avalanche action occurs in small "plasma" columns and the localised heating is excessive. Latching current for the 2N5192 is approximately 10 mA.

For a KD*P Q switch, having a quarter wave retardation voltage of 3.8 kV at 1064 nm, a chain of 20 transistors is required. From the histogram data of figure 3, the chain would operate between 3.2 kV and 4.5 kV, thus allowing some adjustment either side of the nominal quarter wave voltage.

3.1 Voltage rise time

An equivalent circuit for the chain is shown in figure 5 with a capacitive load (C) and stray inductance (L_s). The chain is assumed to have a source resistance R_s in the on state. The effect of stray inductance is to generate a back e.m.f. opposing the voltage change across the capacitive load of

$$V = L_s \frac{di}{dt}$$

The circuit will ring at a frequency of

$$\omega^2 = \frac{1}{L_s C}$$

from which the stray inductance can be obtained as

$$L_s = 1/\{(2\pi f)L2C\} = (T_c)^2/(4\pi^2 C)$$

where T_c is the period of the ringing cycle.

A typical result is shown in figure 6, the rise time and ringing cycle are shown for a tightly packed 6 transistor chain with a 1000 pF load.

The voltage rise time is

$$\tau_{v\ (10\% - 90\%)} = 26 \text{ ns}$$

and the period of the ringing cycle is

$$T_c = 56 \text{ ns}$$

giving

$$L_s = 0.079 \ \mu H$$

It was further noted that the rise time was directly related to the ringing cycle period. The mean over 23 readings gives

$$\tau_v = 0.45\ T_c$$

Table 2 gives the measured results for a single transistor, with no attempt to minimise stray inductance. The last figure in the table is for a 1000 pF capacitor connected with short leads directly across the transistor. This should be compared to the first figure giving the result for a 1000 pF capacitor with its leads intact. A significant reduction in stray inductance could be made with short leads.

TABLE 2. THE EFFECT OF A CAPACITIVE LOAD ON A SINGLE TRANSISTOR

	Capacitor C	Rise time τ_v	Ringing cycle period T_c	$\frac{\tau_v}{T_c}$	Stray inductance L_s
	(pf)	(ns)	(ns)		(μH)
	1000	36	80	0.45	0.162
	470	28	52	0.54	0.146
	330	20	44	0.45	0.149
	220	16	38	0.42	0.164
	150	14	29	0.48	0.142
	82	12	26	0.46	0.209
	47	9	19	0.47	0.195
*	1000	9	18	0.5	0.0082

* Short leads

Table 3 gives the results for a 6 transistor chain, again with no attempt to minimise stray inductance. The rise times are longer and stray inductance higher than for the single transistor. The last figure in Table 3 was obtained when the current rise was limited by a resistive load of 1 KΩ in series with the capacitance as shown in figure 7. The effect of the load resistor is to limit the rate of rise of the current and hence the back e.m.f. The voltage appearing across the load resistor is a fast pulse. For the pulse to be nearly equal in amplitude to the switched voltage, the load resistor should be large compared to the source

resistance. Best results were obtained when the time constant produced by the capacitor and resistor was

$$\tau = RC = 200\ \mu s$$

TABLE 3. THE EFFECT OF A CAPACITIVE LOAD ON A 6 TRANSISTOR CHAIN

	Capacitor C	Rise time τ_v	Ringing cycle period T_c	$\frac{\tau_v}{T_c}$	Stray inductance L_s
	(pf)	(ns)	(ns)		(μH)
	1000	48	106	0.45	0.28
	470	30	76	0.39	0.31
	330	26	60	0.43	0.28
	220	22	50	0.44	0.29
	150	16	38	0.42	0.24
	82	14	31	0.45	0.30
	47	10	25	0.40	0.34
*	1000	8	None		

* with 1 KΩ limiting current

Table 4 gives the results for a 6 transistor chain which was tightly packed in an attempt to minimise stray inductance. Comparison with Table 3 shows that the stray inductance was reduced by a factor of 4. The last figure of Table 4 indicates a stray capacitance of 17.8 pF using the mean inductance to calculate the capacitance. This is considerably higher than the nominal capacitance of the high voltage probe (3 pF) used for the measurements. Hence the probe did not unduly influence the results.

TABLE 4. THE EFFECT OF A CAPACITIVE LOAD ON A TIGHTLY PACKED CHAIN

	Capacitor C	Rise time τ_v	Ringing cycle period T_c	$\frac{\tau_v}{T_c}$	Stray inductance L_s
	(pf)	(ns)	(ns)		(μH)
	1000	26	56	0.46	0.079
	470	17	38	0.45	0.078
	330	14	30	0.47	0.069
	220	12	25	0.48	0.072
	150	9	18	0.5	0.055
	82	8	15	0.53	0.070
	47	6	11	0.55	0.065
*	0	8	7		

* Probe and stray capacitance only

For Q switching, no special care is needed to eliminate stray inductance as voltage rise times of 8 ns are easily obtained with a resistive load to limit the current. This is much less than pulse evolution times (50 to 100 ns) as required.

For pulse gating or cavity dumping, where a fast high voltage pulse is required, some effort to minimise stray inductance is needed but even here the effects of capacitive loading are minimised by the resistive load across which the fast pulse is developed.

3.2 Optical switching speed

Although the voltage rise times given in Tables 2 to 4 are not better than 8 ns, the optical switching is faster. The transmission of the Q switch as a function of time is

$$T(t) = \sin^2 \{(\pi.t)/(2.\tau_v)\}$$

where $T(t)$ is the transmission as a function of time and τ_v is the voltage rise time.

For the transmission to change from 10% to 90%

$$\tau_T = 0.58\ \tau_V$$

where τ_T is the transmission rise time.

With τ_V = 8 ns, the transmission rise time is

$$\tau_t = 4.6 \text{ ns}$$

Thus the circuit is capable of producing 5 ns FWHM pulses from a laser operated in the pulse transmission mode. This was subsequently confirmed experimentally.

4. ALTERNATIVE CIRCUIT FORMS

The basic avalanche chain may be used in a number of ways depending on the requirements. It can be used for normal Q switching, for operating a PTM laser or as a pulse selector (or gate).

4.1 Q switch circuit

When used for Q switching, a single chain as shown in figure 7 is used. If the Q switch is connected to point 1, a DC bias is provided which is shorted to ground when the chain is fired. If connected to point 2 , the Q switch has no bias and a fast pulse is obtained when the chain is fired. This would be used where it is desired to pulse open the Q switch, bias being provided optically.

4.2 Cavity dump drive circuit

Considerable difficulty was experienced in devising a circuit combining two avalanche chains to operate independently within 100 ns of each other. With fast high voltage transients one might expect that firing one chain would induce the second to fire. I am indebted to Mr C. Flecker of this establishment (since retired) for the basic form of the successful circuit. This is shown in figure 8 in which the two transistor chains are again shown schematically as blocks. Chain A provides DC bias to the Q switch and when fired the bias is removed opening the Q switch. Chain B is capacitively coupled to the Q switch. When the capacitor is charged this side of the Q switch is held at ground potential by the resistive load. When chain B is fired a fast pulse is developed across the resistor, thus closing the Q switch rapidly. Note the resistive load removes the effect of the capacitive coupling as described in the preceding section.

The coupling capacitor used for chain B should be large compared to the Q switch capacitance as these form a capacitive voltage divider. The voltage appearing across the Q switch is

$$V_q = \frac{C_q}{C + C_q}$$

where C_q is the Q switch capacitance and C is the coupling capacitor.

A high voltage diode as shown between chain B and the Q switch can help prevent fast transients from chain A interacting with chain B but is not essential.

This work was previously reported at the 1st Australian National Laser Conference, March 1978. Since then Davis et al(ref.13) have reported on a very similar circuit which was developed for pulse gating.

4.3 Pulse gating

If the Q switch connection to chain A is made between the resistor and capacitor, as for chain B, then no bias appears on the Q switch.

Firing of the two chains with a short delay between them now yields a square pulse which may be used to gate or select one pulse from a pulse train. This is the form of the circuit used by Davis et al.

5. CONCLUSION

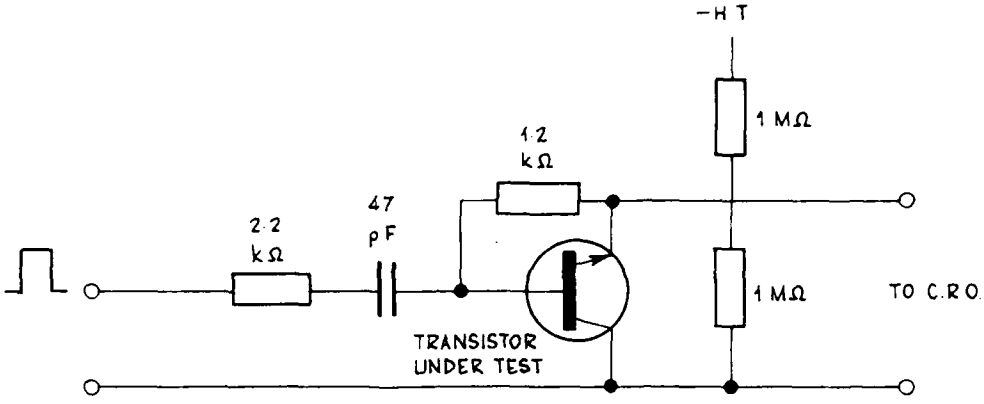
A very reliable avalanche transistor Q switch driver has been designed, based on the 2N5192 transistor. The double chain version has been successfully used to generate 5 ns FWHM pulses from a pulse transmission mode laser.

A single chain version has been used as a Q switch drive for a laser running at 168 Hz for well in excess of 100 hours. No life limitation is foreseen.

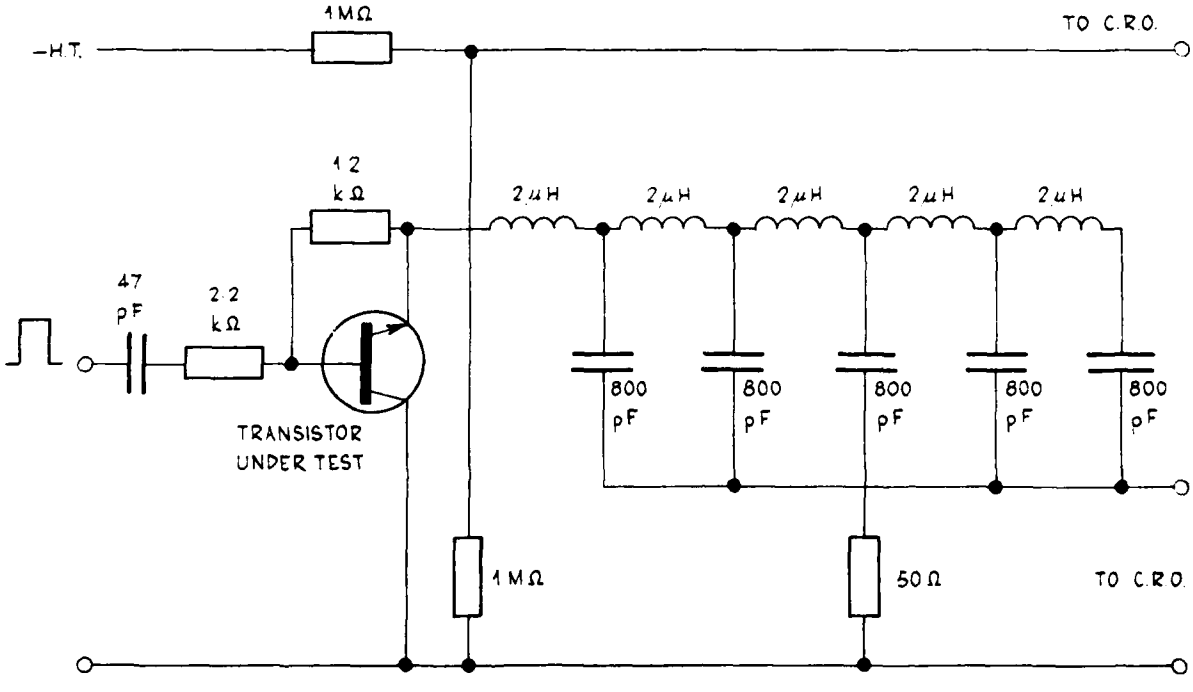
REFERENCES

No.	Author	Title
1	Hook, W.R., Dishington, R.H. and Hilberg, R.P.	"Laser Cavity Dumping using Time Variable Reflection". Applied Physics Letters, V 9, No.3, pp 125 - 127, 1 August 1966
2	Hook, W.R., Hilberg, R.P. and Dishington, R.H.	"A TVR Laser Oscillator using a single pockels cell for Q switching and Synchronised Cavity Dumping". Proceedings of the IEEE, pp 1954 - 1955, December 1966
3	Ley, J.M., Christmas, T.M. and Wildey, C.G.	"Solid State Subnanosecond Light Switch". Proceedings of the Institute of Electrical Engineers, V 117, No.6, pp 1057 - 1062, June 1970
4	Thomas, S.W. and Coleman, L.W.	"Laser Triggered Avalanche Transistor Voltage Generator for a picosecond Streak Camera". Applied Physics Letters, V 20, No.2, pp 83 - 84, 15 January 1972
5	Corcoran, V.J., McMillan, R.W. and Rushworth, P.M.	"Selection of ON Mode-locked Laser Pulses". Applied Optics, V 14, No.3, pp 643 - 646, March 1975
6	Brasseur, G., Van Eck, J.L. and Vilain, P.	"Selection of a single pulse from a mode-locked laser using avalanche transistors". Applied Optics, V 14, No.8, pp 1758 - 1759, August 1975
7	Harney, R.C.	"Pockels Cell Pulse Stackers". Lawrence Livermore Laboratory, Ucrl 51908, 7 January 1976
8	Henebry, W.M.	"Avalanche Transistor Circuits." Review of Scientific Instruments. V 32, No.11, pp 1198 - 1203, November 1961
9	Bell, B.H.	"Avalanche circuits are more Versatile than you Think". Electronic Design, pp 56 - 61, 8 June 1964
10	Bramson, M.	"Application of Avalanche Transistors to 10 Megacycle Pulse Generators". IRE Transactions on Nuclear Science, pp 35 - 37, August 1962

No.	Author	Title
11	Miller, S.L. and Ebers, J.J.	"Alloyed Junction Avalanche Transistors". Bell System Technical Journal, V 34, No.5, pp 883 - 902, September 1955
12	See, B.A.	"A Pulse Transmission Mode Laser". 1st Australian National Laser Conference, March 1978
13	Davis, S.J., Murray, J.E. Downs, D.C. and Lowdermilk, W.H.	"High Performance Avalanche Transistor Switchout for external Pulse selection at 1.06 nm." Applied Optics, V 17, No.19, pp 3184 - 3186, October 1978



(a) Basic test circuit



(b) Pulse test circuit

Figure 1. Test circuits for Avalanche transistors

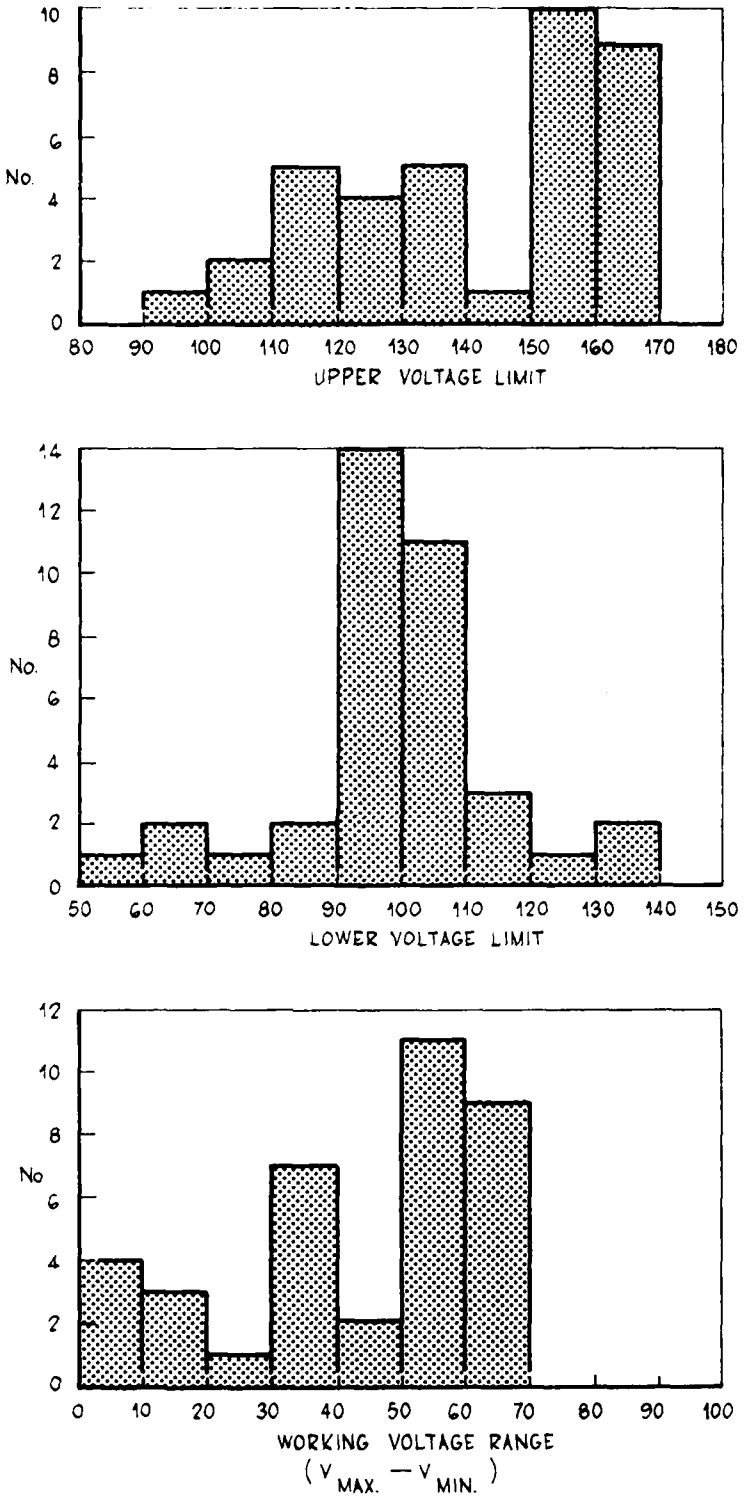


Figure 2. 2N2222 Avalanche characteristics

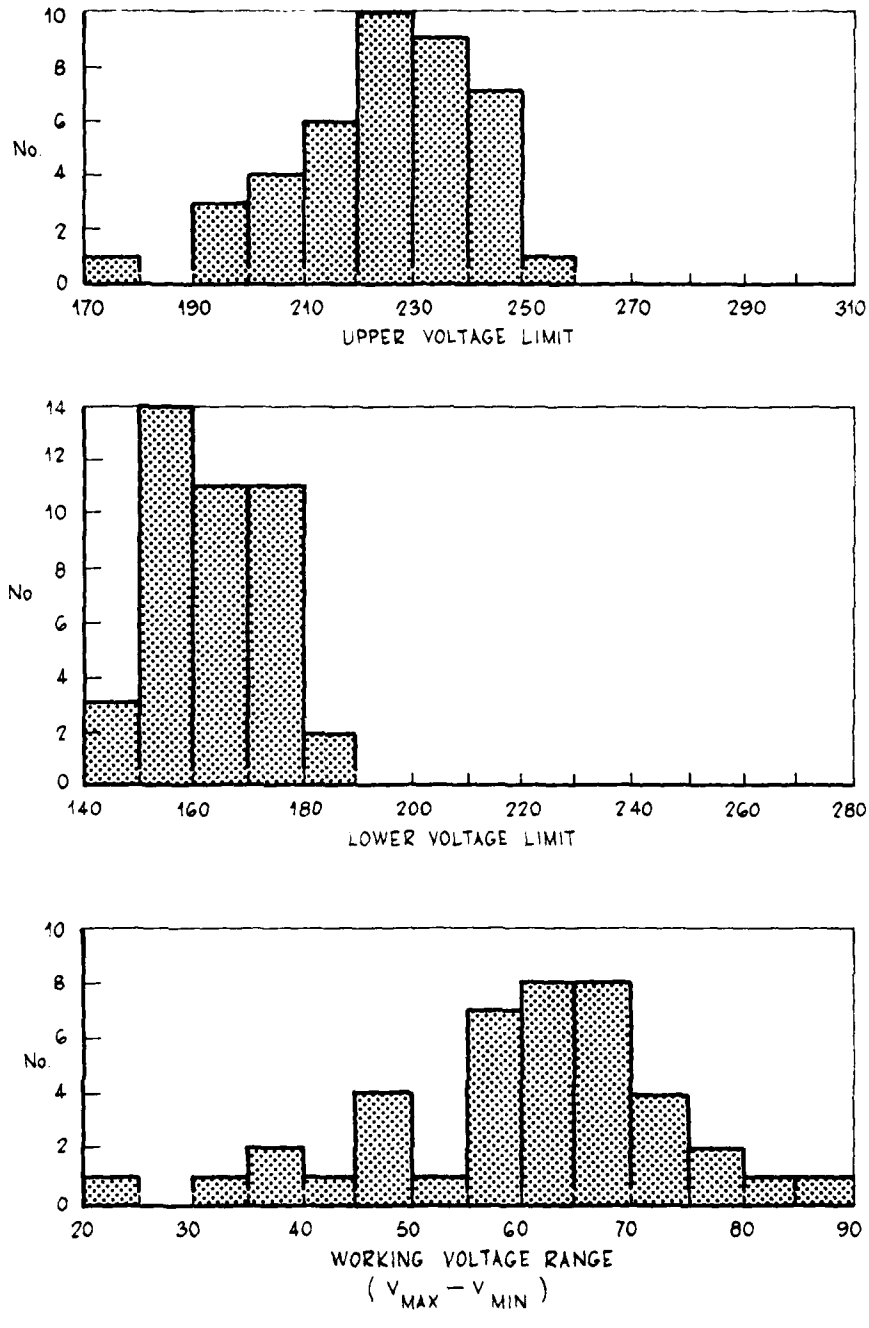


Figure 3. 2N5192 Avalanche characteristics

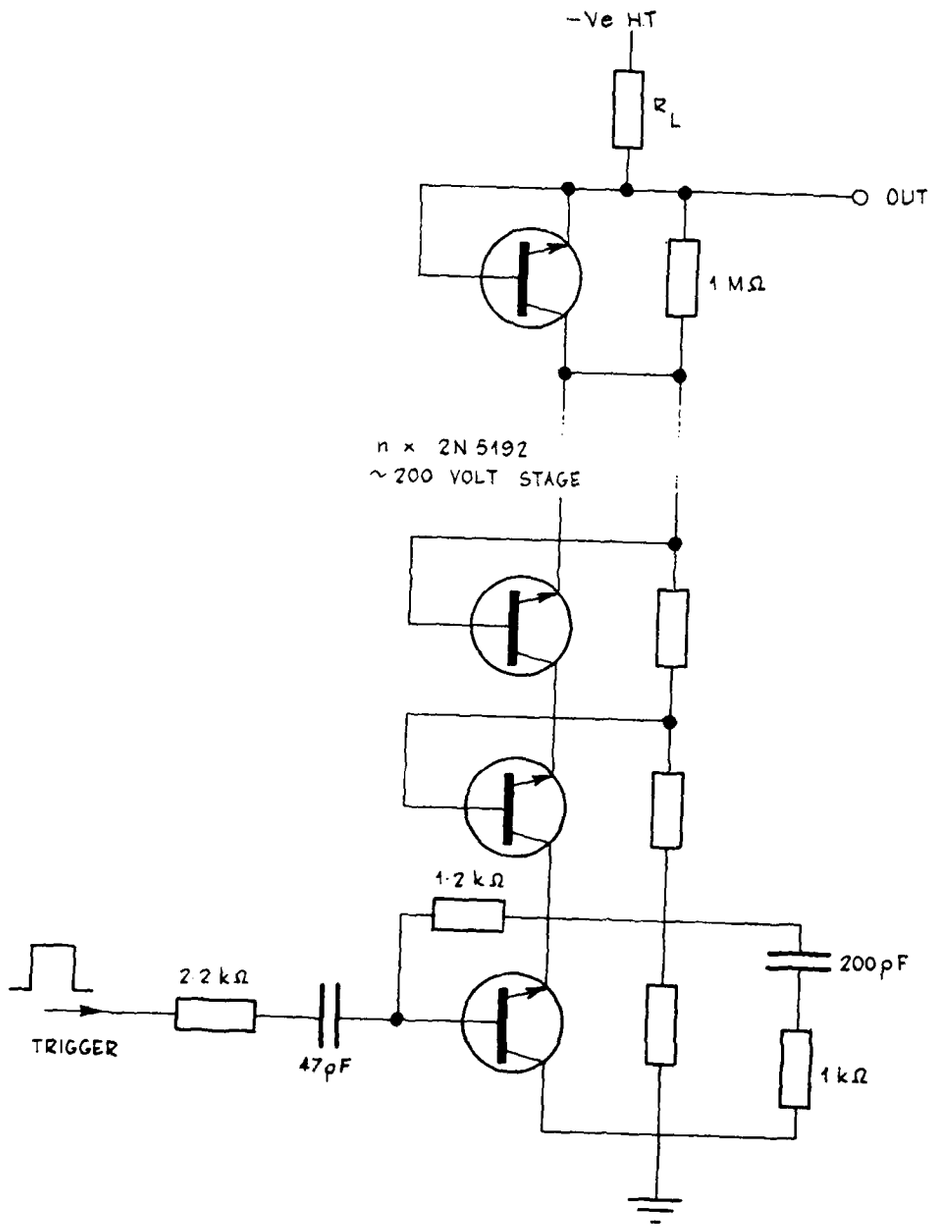


Figure 4. Avalanche transistor chain

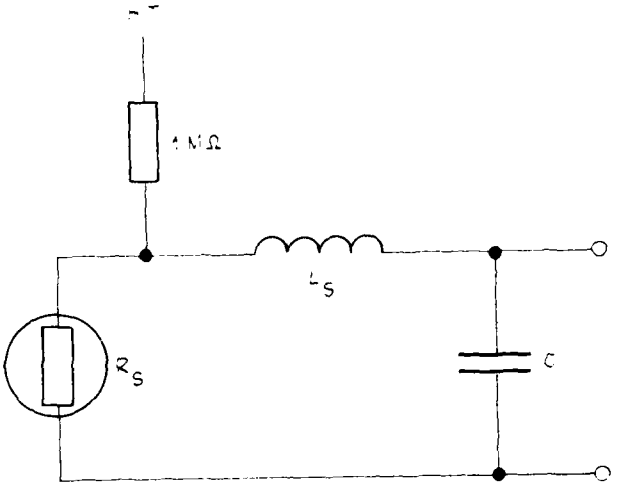


Figure 5. Equivalent circuit in ON state

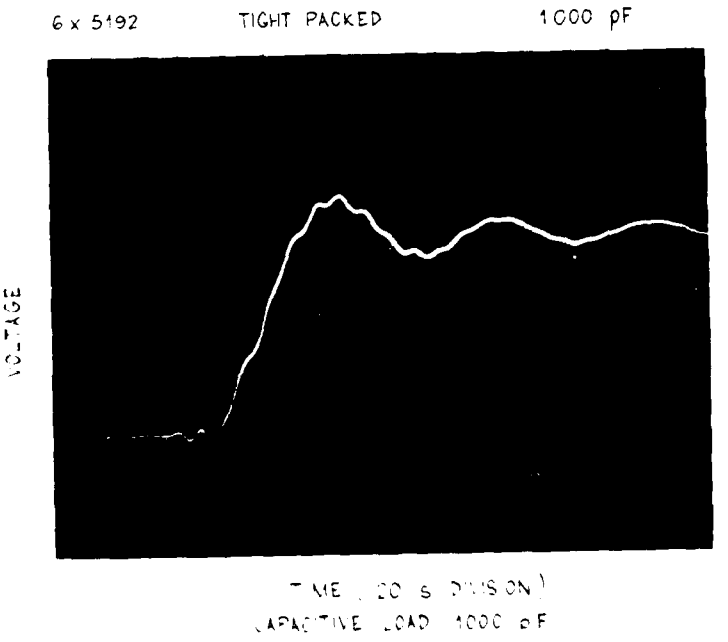


Figure 6. Voltage step for 6 transistor chain

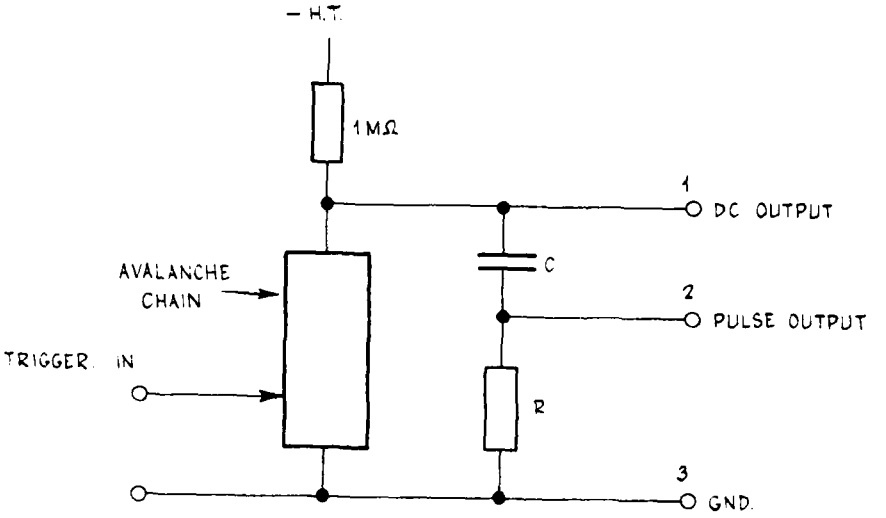


Figure 7. Circuit for pulse output

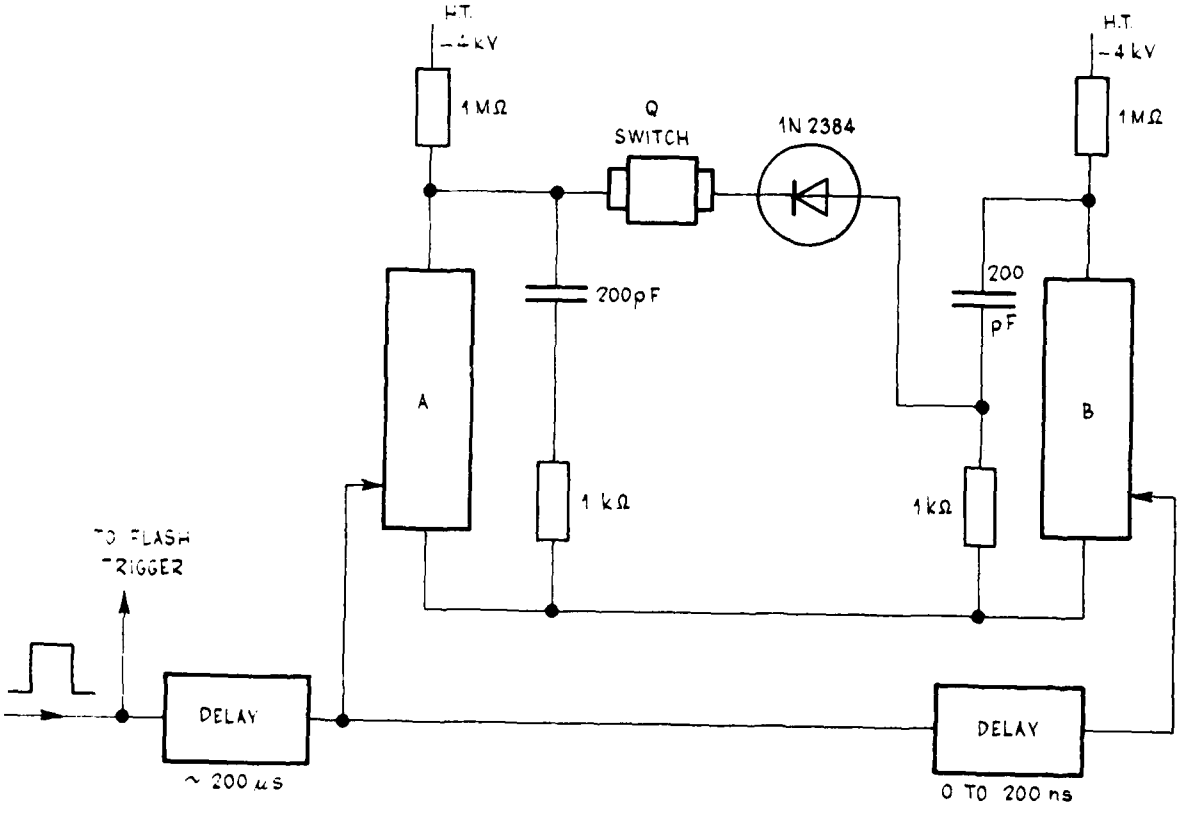


Figure 8. PTM Q switch drive circuit

DISTRIBUTION

	Copy No.
EXTERNAL	
In United Kingdom	
Institution of Electrical Engineers Hitchin Herts England	1
British Library Lending Division Boston Spa, Yorkshire, England	2
Technology Reports Centre Orpington Kent England	3
In United States of America	
National Technical Information Service Springfield, Va. USA	4
NASA Scientific & Technical Information Office Washington DC USA	5
Engineering Societies Library New York NY USA	6
Cambridge Scientific Abstracts Riverdale Md USA	7
In Australia	
Chief Defence Scientist	8
Deputy Chief Defence Scientist	9
Controller, Projects and Analytical Studies	10
Superintendent, Major Projects	11
Superintendent, Science and Technology Programmes	12
Defence Information Services Branch (for microfilming)	13
Defence Information Services Branch for:-	
United Kingdom, Ministry of Defence, Defence Research Information Centre (DRIC)	14
United States, Department of Defense, Defense Documentation Center	15 - 26
Canada, Department of National Defence, Defence Science Information Service	27
New Zealand, Ministry of Defence	28
Australian National Library	29
Defence Library, Campbell Park	30

Library, Aeronautical Research Laboratory 31

Library, Materials Research Laboratory 32

Director, Joint Intelligence Organisation (DDSTI) 33

WITHIN DRCS

Chief Superintendent, Electronics Research Laboratory 34

Superintendent, Navigation and Surveillance Division 35

Principal Officer, Laser Group 36

Principal Officer, Optical Techniques Group 37

Principal Officer, Terminal Guidance Group 38

Principal Officer, Control and Instrumentation Systems Group 39

Principal Officer, Mechanisms and Instrumentation Group 40

Mr M.F. Penny, Laser Group 41

Mr C. Lowe, Terminal Guidance Group 42

Dr J. Richards, Laser Group 43

Dr R. Seymour, Laser Group 44

Dr D. Phillips, Laser Group 45

Mr D. Rees, Laser Group 46

Mr K. Fueloep, Laser Group 47

Mr P. Wilsen, Laser Group 48

Mr C. Lightowler, Control and Instrumentation Systems Group 49

Mr C. McIntosh, Control and Instrumentation Systems Group 50

Mr D. Taylor, Terminal Guidance Group 51

Mr N. Irwin, Terminal Guidance Group 52

Author 53 - 58

DRCS Library 59 - 61

Spares 62 - 65

The official documents produced by the Laboratories of the Defence Research Centre Salisbury are issued in one of five categories: Reports, Technical Reports, Technical Memoranda, Manuals and Specifications. The purpose of the latter two categories is self-evident, with the other three categories being used for the following purposes:

Reports	:	documents prepared for managerial purposes.
Technical Reports	:	records of scientific and technical work of a permanent value intended for other scientists and technologists working in the field.
Technical Memoranda	:	intended primarily for disseminating information within the DSTO. They are usually tentative in nature and reflect the personal views of the author.