NRL Report 6539

A Nanosecond, High-Current Pulse Generator Using Paralleled Avalanche Transistors

September 8, 1967

NAVAL RESEARCH LABORATORY
Washington, D.C.

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A Nanosecond, High-Current Pulse Generator Using Paralleled Avalanche Transistors

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ABSTRACT

A nanosecond, high-current pulse generator using paralleled avalanche transistors has been designed, and its operating characteristics have been determined. The generator utilizes the regenerative switching action of avalanching transistors to discharge capacitors through a low-impedance load. Transistors are selected for high collector-to-base diode breakdown voltage, BV_{CBO}, low avalanche latching voltage, LV_{CER}, and fast avalanche switching. Control of the switching times of individual avalanche transistors is achieved by adjusting collector bias levels. This technique allows a variety of pulse waveforms to be generated, including pulse groups with adjustable pulse-to-pulse spacings. Output pulse waveforms are characteristic of a slightly underdamped RLC series circuit.

Two models of the generator were developed using standard transistors and components. Peak pulse currents on the order of 40 amperes, with rise time less than 10 nsec and repetition rates greater than 10 kHz, were produced in loads of approximately one ohm. The generators are suitable for pulse modulating low-impedance devices such as GaAs room-temperature injection lasers.

PROBLEM STATUS

This is an interim report; work on the problem is continuing.

AUTHORIZATION

NRL Problem R02-14
Project RF 001-02-41-4005

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A NANOSECOND, HIGH-CURRENT PULSE GENERATOR USING PARALLELED AVALANCHE TRANSISTORS

INTRODUCTION

In systems employing electro-optical devices such as the GaAs room-temperature laser diode, it is often necessary to produce narrow, high-current pulses for driving a sub-ohmic load impedance. The most practical pulse-generation technique for this application utilizes the triggered-switch, capacitance-storage configuration (1a) shown in Fig. 1. When the switch is in a high-impedance "off" state, the capacitor C_1 assumes a charge through the resistor R_1. If the switch is triggered into a low-impedance "on" state, C_1 will discharge through the load. After the voltage across C_1 has dropped to a low level, the switch returns to the "off" state, and C_1 recharges. Electromechanical switching elements are often used in this type of circuit in order to produce the large-amplitude, fast-rise pulses required for diode laser modulation (2,3). These types of switches have the disadvantages of low pulse-repetition frequency (typically less than 1000 pps), and considerable pulse-amplitude and time jitter (1b).

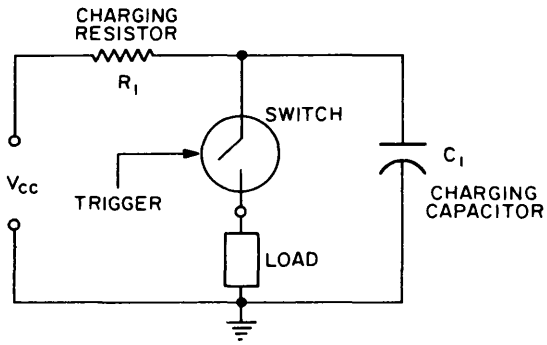


Fig. 1 - Pulse-generator configuration; triggered switch, capacitance storage

Extensive capacitance-storage pulse circuitry has been developed using the avalanche-multiplication property of silicon transistors as the switching mechanism (4-7). A silicon high-frequency transistor can exhibit a triggered avalanche-switching time of the order of one nanosecond, with negligible pulse-to-pulse jitter. The pulse-repetition frequency is limited by power dissipation, but for narrow high-current pulses it can be as great as 5 Mpps in a simple avalanche circuit (8a). Typically, peak current amplitude through the avalanche switch is limited to approximately 20 amperes by an effective avalanche collector spreading resistance, r_{ce} (9).

A low-threshold GaAs injection laser may require narrow current pulses with a peak current of the order of 30 amperes.* Thus, a single transistor in avalanche is usually not adequate as the current-switching device. Experiments have been performed (1c,5,7), however, in which multiple-avalanche transistor switches were paralleled to share the load requirements and produce higher peak currents. The main difficulty encountered in paralleling avalanche transistors to generate short, high-current pulses has been in synchronizing the individual switching times (1c,5). The present report describes the design of a paralleled avalanche-transistor pulse generator in which switching synchronization is achieved by adjustments of the collector bias levels. This technique allows pulse groups to be generated and gives some control over pulse waveshape.

*Low threshold injection lasers made by the solution regrowth method.

In order to fulfill a requirement for a diode laser pulse modulator, two paralleled-stage avalanche-transistor pulse generators were designed and developed utilizing type 2N3020 transistors and standard components. The primary requirements for the generator were a positive pulse current greater than 25 amperes (into a one-ohm load), a pulse rise time* less than 5 nsec, a pulse duration† less than 15 nsec, and a repetition rate of 10 kpps. Compactness and simplicity of operation were important design factors.

BASIC DESIGN

Static terminal characteristics (10) of a transistor which may operate in the avalanche mode are similar to those shown in Fig. 2. An avalanche negative-resistance region enables the transistor to act as a regenerative switching device. The general theory of avalanche multiplication has been examined quite comprehensively by other authors (6,8b,11) and will not be discussed in this report.

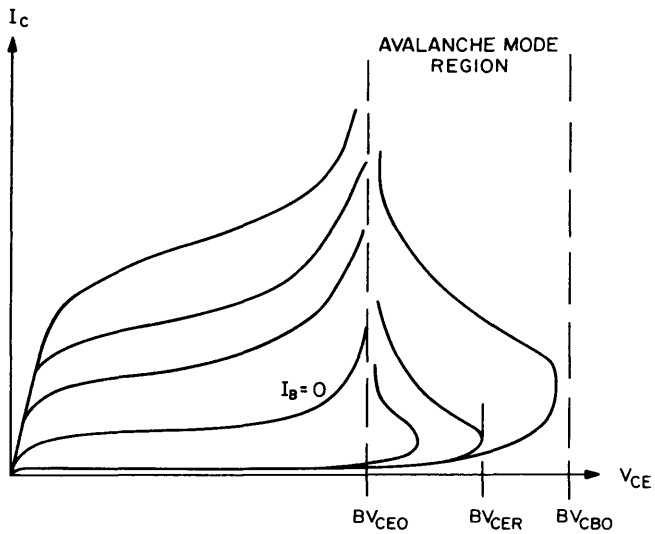


Fig. 2 - Static terminal characteristics of a transistor which may operate in the avalanche mode

Selection of an Avalanche Transistor

Initial design of the elementary avalanche pulse generator requires the selection of a transistor which will operate effectively in the avalanche mode. The basic requirement for transistor avalanche multiplication is that there be a significant difference between the collector-to-base diode breakdown voltage, BV_{CBO}, and the avalanche latching voltage, LV_{CER}. Several types of silicon NPN transistors were tested, and all were found to avalanche to some degree (see Table 1 for a comparison of several transistor types).

The transistor finally selected was the (Motorola) 2N3020, both because of its high-amplitude output (a single stage 2N3020 pulse generator may produce pulses with amplitudes greater than 80 V across a 50-ohm load) and because of the general uniformity of avalanche characteristics between transistor units.

*Pulse rise time t_r measured from 10 to 90 percent peak amplitude.
†Pulse duration t_d measured from 50 to 50 percent peak amplitude.

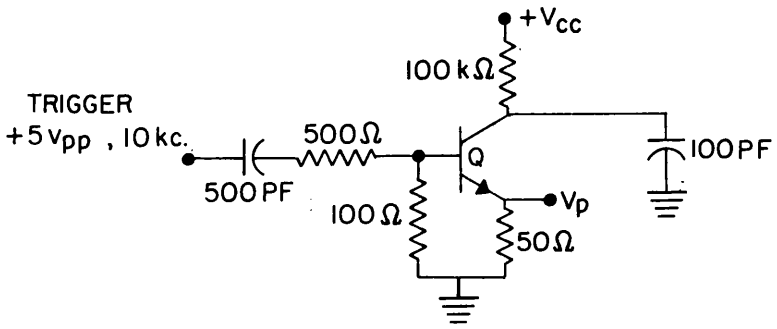


Table 1
Comparison of the Avalanche Pulse Produced by
Several Types of Silicon NPN Transistors

Transistor Type	Bias Level V_{CC} (volts)	Rise Time t_r (nsec)	Duration t_d (nsec)	Avalanche Pulse V_p (volts)
2N657	230	4	≃ 10	94
2N697	140	3		65
2N706	58	3		23
2N3019	175	2		71
2N3020	180	2		80

Design of the Elementary Avalanche Transistor Pulse Generator

An elementary pulse-generating circuit using the common-emitter configuration is shown in Fig. 3. The minimum value of the collector bias resistor R_1 is determined by the static load line, $I_c = (V_{cc} - V_c)/(R_1 + R_L)$, which must be situated below the low-voltage breakdown curve in order to prevent latching and thermal destruction. A general minimum value for R_1 may be calculated from (12): $R_1 \geq (V_{CC} - 20) \times 10^2$. If V_{CC} is 220 V, minimum R_1 is approximately 20 k. The base resistance R_B is necessary to limit the collector current density before avalanche (13), but should be kept as small as possible in order to minimize the effect of the collector-to-base transition capacitance. Practical values for R_B usually range from 10 to 100 ohms. The charging capacitor C_1 must be of sufficient capacitance to provide the maximum pulse current through the load yet be

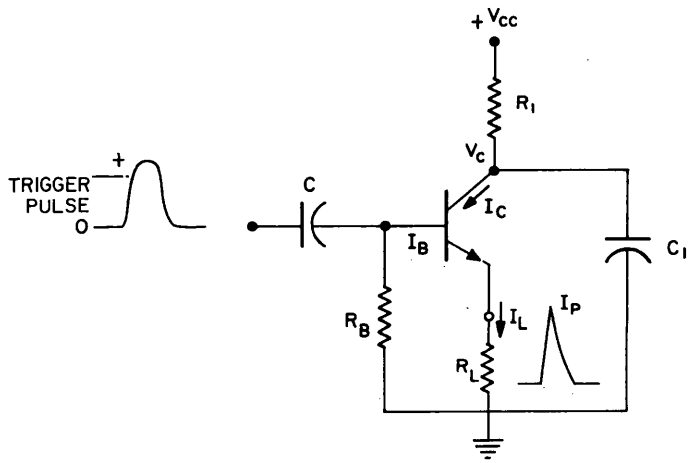


Fig. 3 - Elementary avalanche
transistor pulse generator

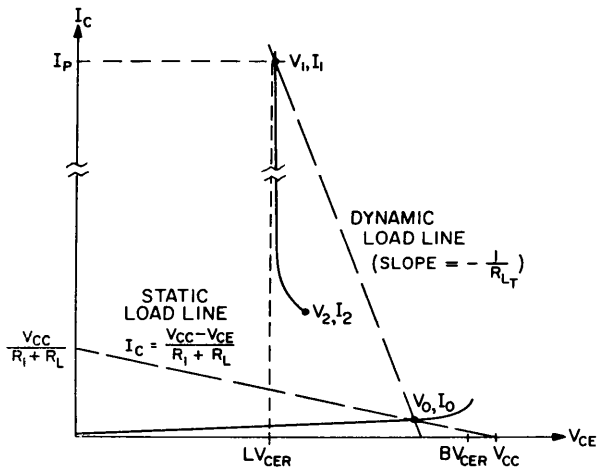
small enough to produce a short pulse-decay time. If the pulse duration is negligible in comparison with the time between trigger pulses, the maximum repetition period for separate avalanche pulses is limited by the recharging time constant R_1C_1. If R_1 = 20 k and C_1 = 1000 pf, the maximum recharging rate of the basic circuit is approximately 50 kHz.

The pulse output from the basic circuit, assuming no series inductance, may be determined by examining the static and dynamic load-line intersections on the common-emitter characteristics of the avalanche transistor (Fig. 4a). The transistor is quiescently biased at point V_0, I_0 on the static load line. The position of this operating point determines the magnitude of the positive trigger pulse required to cause avalanche. For a given bias resistor R_1, the intersection of the static load line with the first avalanche curve may be moved in relation to the avalanche condition by varying the collector bias, V_{CC}. If a sufficiently large positive voltage pulse is applied at the base junction, negative base current will effectively increase and drive the transistor into the negative-resistance portion of the avalanche region. The voltage step that is available to the load is determined by the intersection of the dynamic load line with the breakdown curve at point V_1, I_1. (The general slope of the dynamic load line is $-(1/R_{LT})$, where $R_{LT} \approx R_L + r_{ce}$.) Collector current through the transistor is constrained by the avalanche breakdown curve from point V_1, I_1 to point V_2, I_2. At point V_2, I_2, collector current becomes insufficient to maintain avalanche, and the transistor drops out of the "on" state. Condenser C_1 (Fig. 3) recharges through R_1 as the transistor returns to the quiescent state at point V_0, I_0.

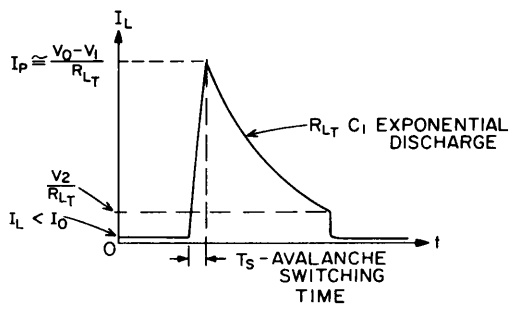
The current switched through the load resistance has the general waveshape shown in Fig. 4b. Maximum pulse current is determined by the avalanche difference voltage $V_0 - V_1$. The exponential decay of this current is controlled by the $R_{LT}C_1$ time constant. When the collector current reaches I_2, the transistor switches "off" and the load current returns to a quiescent level which is much less than I_0.

The Discharge Circuit

The effect on the pulse output of series inductance in the discharge loop may be illustrated by examining the RLC circuit in Fig. 5a. The discharge of current through R_L after the switch is closed will be as shown in Fig. 5b. For the ideal case, when series inductance is not present, the waveshape is that of an RC circuit, with rise time being determined by the actual transition time of the switch.



a. Static and dynamic load lines



b. Load current versus time

Fig. 4 - Characteristics of the elementary avalanche pulse generator

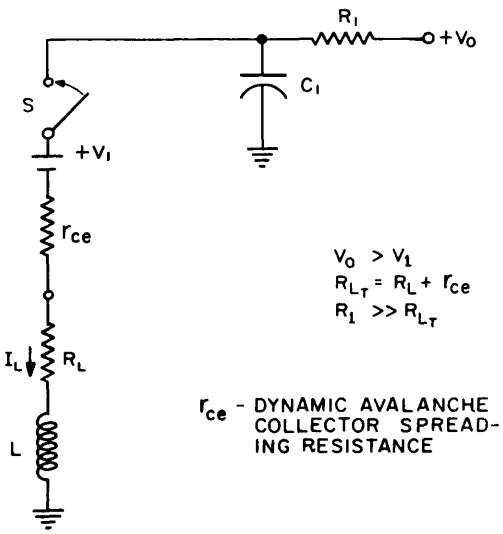
If series inductance is included in the circuit, rise time and peak current amplitude are degraded according to the relative magnitudes of series resistance R, inductance L, and capacitance C.

An expression for the time dependent discharge current through R_L will be of the form,

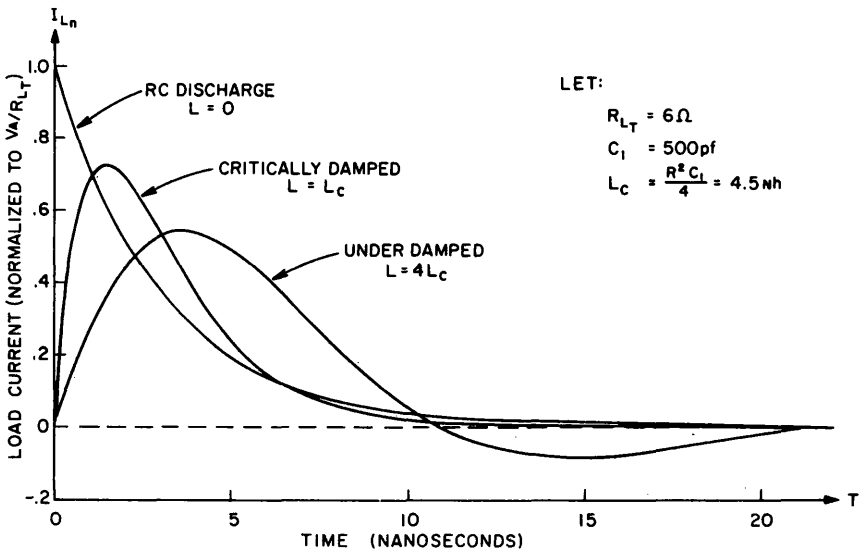
$$i_{(T)} = \frac{(V_0 - V_1)}{L} \frac{1}{(S_1 - S_2)} (e^{S_1 T} - e^{S_2 T}),$$

where

$$S_1 = -\frac{R}{2L} + \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}}, \quad S_2 = -\frac{R}{2L} - \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}},$$



a. RLC circuit with a switch



b. Load current versus time in the RLC circuit

Fig. 5 - Characteristics of RLC discharge circuit

If $R > 2\sqrt{L/C}$, the mathematical values of S are real, and the current will rise to a maximum and then gradually die away in a single unidirectional surge. This is known as the overdamped response (14). The underdamped, or oscillatory, response occurs when $R < 2\sqrt{L/C}$, causing the values of S to be imaginary. In this case the current rises to a maximum, falls, reverses its direction of flow, then reverses again, continuing to oscillate periodically with decaying amplitude until it eventually dies out. A special mathematical case occurs for $R = 2\sqrt{L/C}$, when the oscillatory response merges into the overdamped response. This condition is termed the critically damped response (14). Thus, for a given series loading resistance R_L and charging capacitance C_1, the waveshape of the pulse output of the simple avalanche circuit will be limited by two factors: the total series inductance in the discharge circuit, and the actual avalanche switching characteristics of the transistor.

As an example, the avalanche switching time of a high-frequency transistor may be less than 1 nsec. If the dynamic collector spreading resistance r_{ce} is assumed to be five ohms, with C_1 equal to 500 pF and R_L equal to one ohm, then the critical inductance L_C is 4.5 nH. Load-current waveshapes are shown in Fig. 5b for values of L near L_C. Notice that, for the critically damped condition, $L = L_C$, pulse rise time has been increased to 1 nsec and peak pulse amplitude has been reduced by 28 percent as compared to a pure RC discharge circuit. When L is greater than L_C, negative transients are produced and rise time and amplitude are degraded to a still greater degree.

It is desirable to minimize negative transients, since they may cause overheating in a diode laser. Unfortunately, stray series inductance in a lumped RC circuit, even with good high-frequency construction techniques, will be of the order of a few nanohenries (1c). The value of either R_L or C_1 should, therefore, be kept large enough to prevent the underdamped condition. A tradeoff in pulse amplitude or duration is involved, since an increase in R_L will cause a decrease in peak pulse current, while an increase in C_1 will increase the pulse decay time.

Paralleled Avalanche Transistor Switches

Consider the case of multiple RLC switch circuits paralleled across a common load (Fig. 6a). Theoretically, with identical component parameters and unidirectional switches, the switches can be triggered at the same time, and the total output current will retain the individual stage rise time and duration, but with increased amplitude (Fig. 6b). In this ideal case each switch shares part of the load, with no degradation of output waveshape.

The major problem associated with paralleling avalanche transistors is in triggering the transistors to switch at exactly the same time. Variations in avalanche characteristics cause the individual transistors to avalanche at slightly different trigger voltage levels. As shown in Fig. 6c, differences in switching times result in decreased amplitude and increased rise and fall times.

The problem of avalanche switch synchronization is usually solved by using selected transistors with matched avalanche characteristics, by inserting individual delay lines in both the base-trigger and emitter-to-load circuits, or by shaping the input trigger pulses (5,7). These solutions restrict the replacement of transistor units and usually require critical circuit layouts. It is also difficult to match delay lines with low-impedance loads.

Paralleled transistor switches can be synchronized by adjusting individual transistor collector bias. In this manner, transistors with slightly different avalanche characteristics may be biased so as to switch at the same trigger voltage. This biasing method also provides a means of generating pulse groups with variable pulse-to-pulse delays within the group. The delays are controlled by biasing the individual transistors to switch at selected voltage levels of a comparatively slowly rising trigger pulse. Each transistor

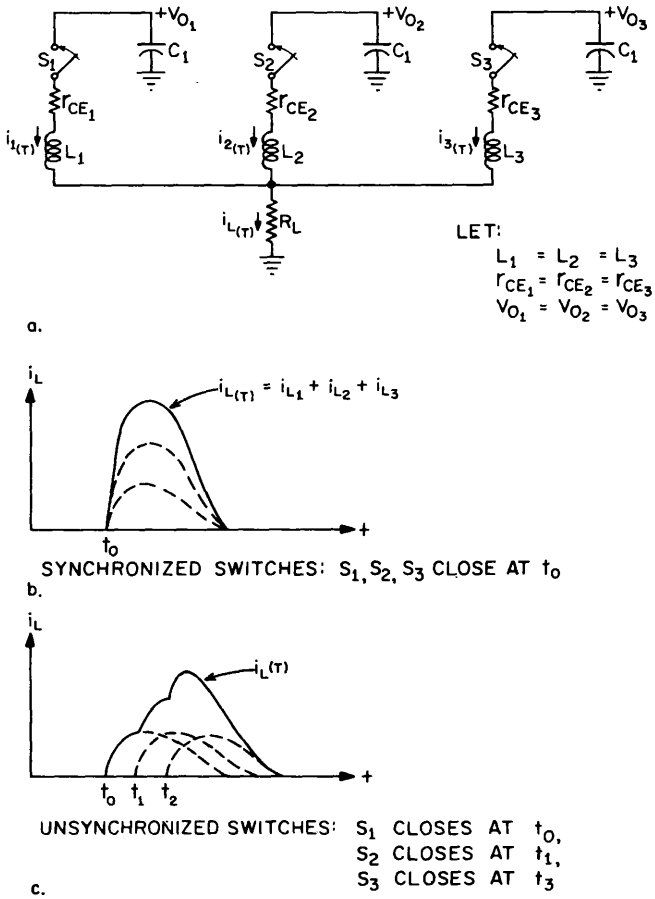


Fig. 6 - Paralleled RLC circuits with switches

acts as a level detector, with the delays between avalanche pulses corresponding to the time intervals between the switching voltages on the leading edge of the trigger pulse (Fig. 7). The maximum delay between the first and last pulse of the pulse group is limited to the trigger-pulse rise time. As shown in Fig. 8, the delaying technique can be used to eliminate negative transients following the main output pulse. A transient may be cancelled out by means of a single avalanche transistor generator whose positive output pulse is delayed to coincide with the negative transient.

One disadvantage inherent in varying bias is that a change in collector voltage will cause a change in output pulse amplitude and rise time. It was found, however, that the slight bias adjustments needed for time synchronization did not have an appreciable effect on the pulse waveforms of individual transistor generators.

Completed Pulse Generators

Two avalanche transistor pulse generators were constructed and tested. Schematics of both generators are shown in Fig. 9. Model A (Figs. 9a and 10a,b) is a five-transistor pulse generator which utilizes a 2N706 transistor in self-oscillating avalanche as the trigger generator for four paralleled 2N3020 transistors. The charging circuitry for the paralleled avalanche transistors consists of four 500-pF ceramic button capacitors

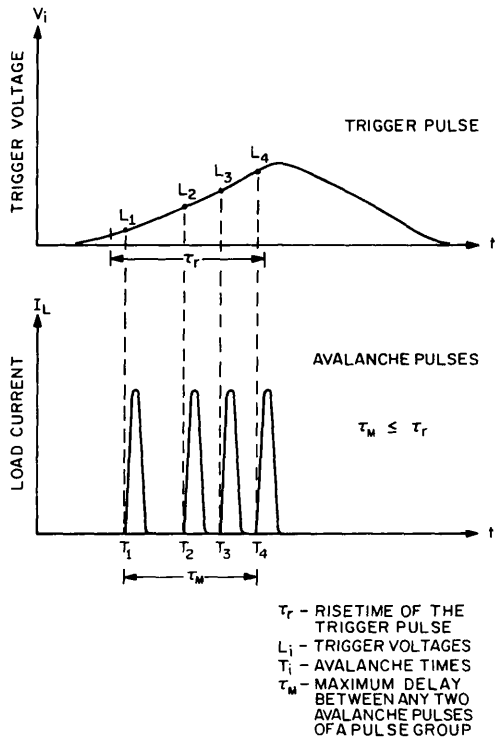


Fig. 7 - Control of pulse-to-pulse delays by selection of trigger levels

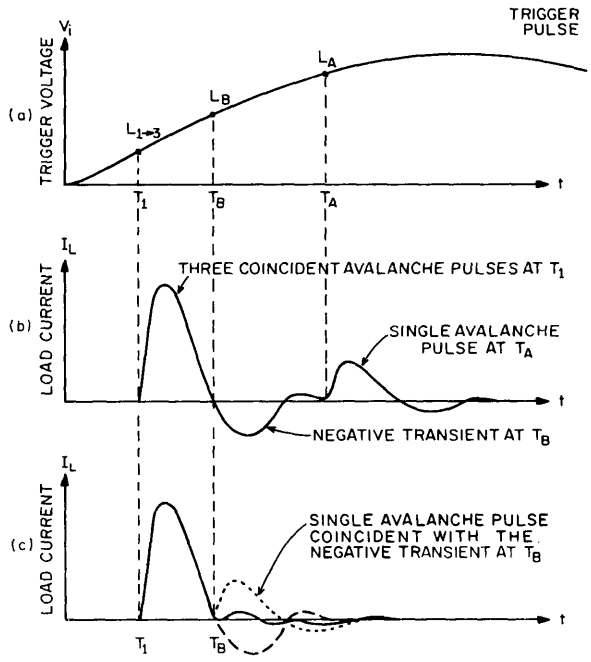
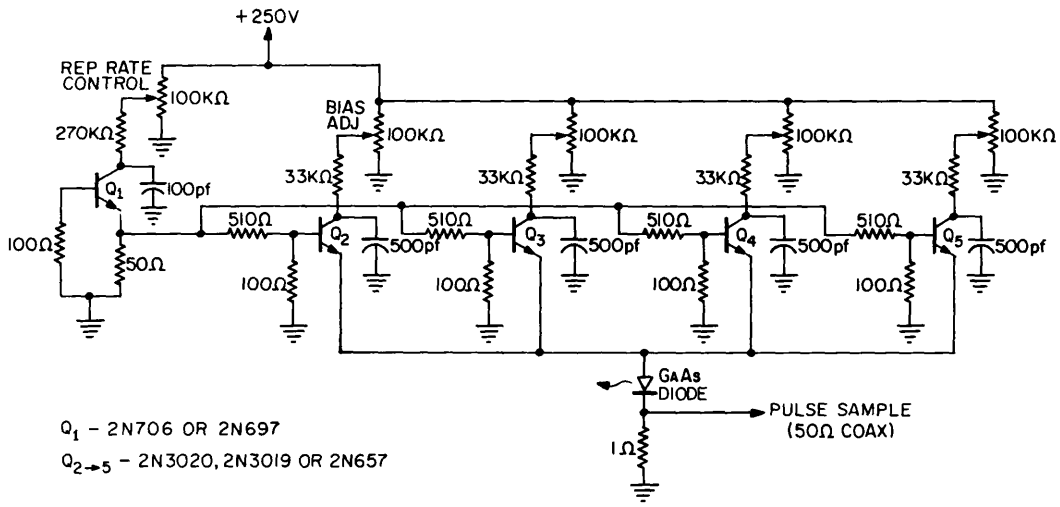
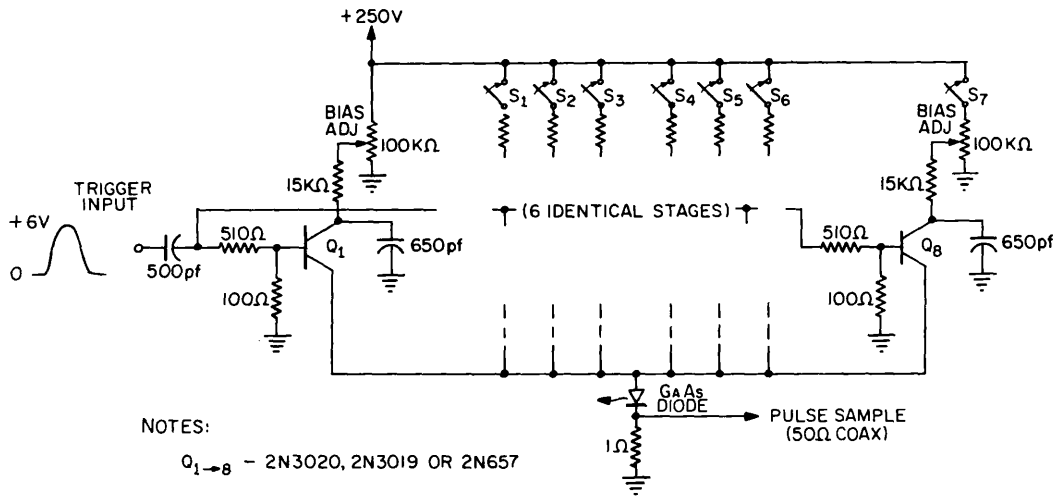


Fig. 8 - A technique for canceling a negative transient. Upper curve: trigger-pulse voltage; center curve: main pulse with a negative transient triggered at T_1 by voltage level L_1; lower curve: the voltage level triggering a single avalanche pulse is adjusted from L_A to L_B, causing the positive pulse to coincide with the negative transient at T_B.



a. Model A

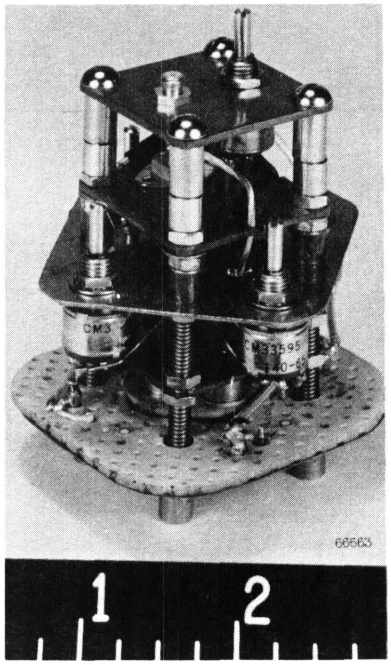


b. Model B

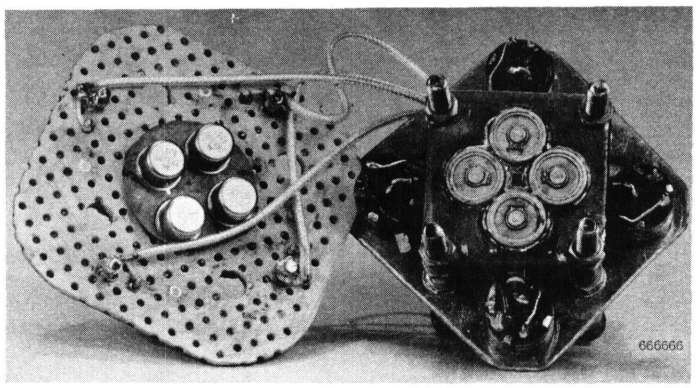
Fig. 9 - Pulse-generator schematic

soldered to a copper plate. Electrical contact to the collectors of the transistors is made by a pressure fit between the center conductor of the capacitor and the transistor header (which is tied to the collector). All lead lengths in the discharge circuit were kept as short as possible in order to minimize series inductance. The 2N706 avalanche oscillator produces a 20-V_{PP}, 20-nsec positive trigger pulse. Repetition rate may be varied between 5 kpps and 15 kpps by changing the bias level. Avalanche synchronization of the paralleled 2N3020 transistors is controlled by adjusting four voltage dividers at the collector bias terminals.

A variety of pulse waveforms, including a single maximum-amplitude pulse (Fig. 11a) and a group of three pulses (Fig. 11c), may be generated. The model A pulse generator can produce a very clean, 25-ampere, 4-nsec rise-time, 8-nsec-duration current pulse



a. Complete pulse-generator assembly

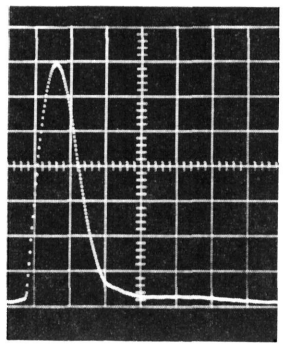


b. Transistors and charging capacitors

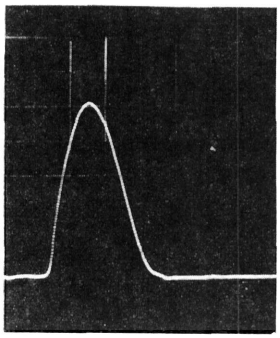
Fig. 10 - Construction of the model A pulse generator

(Fig. 11b) in a laser diode in series with a one-ohm sampling resistor. Pulse amplitude may be increased in approximately eight-ampere steps from 8 to 35 amperes by allowing a total of one through four transistors to avalanche synchronously. The model A pulse generator has been successfully used to drive a GaAs injection laser diode having a room-temperature threshold of 22 amperes.

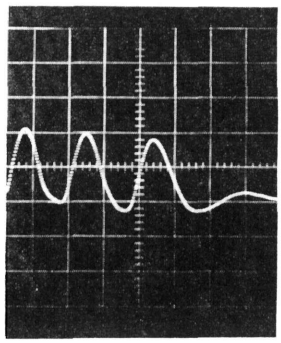
The model B pulse generator was designed and constructed when it became necessary to produce slightly higher peak current pulses with a finer provision for pulse-amplitude control. Model B (Figs. 9b and 12a-c) is an externally triggered pulse generator which uses eight paralleled 2N3020 transistors. The required trigger input for single-pulse operation is a positive 6-V, 100-nsec-rise-time pulse at a repetition rate of



a. Single maximum current pulse, r.t. 6 nsec, duration 10 nsec, amplitude 35 A; vertical scale 5 A/div., horizontal scale 10 nsec/div.



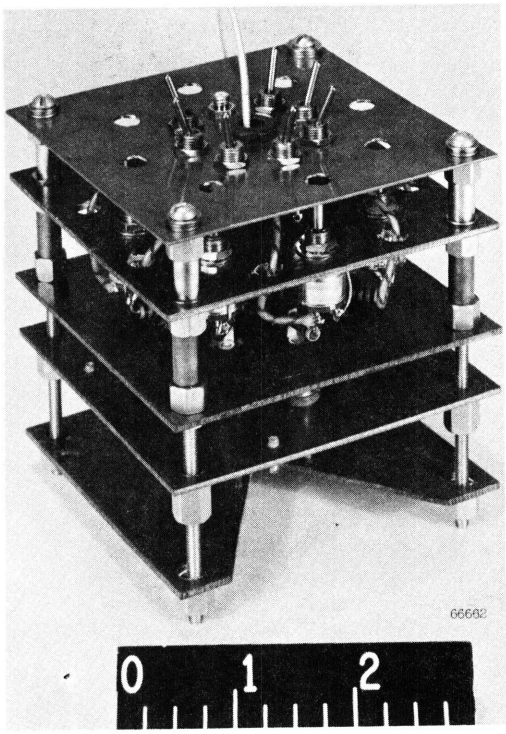
b. Single pulse, r.t. 4 nsec, duration 8 nsec, amplitude 25 A; vertical scale 5 A/div., horizontal scale 5 nsec/div.



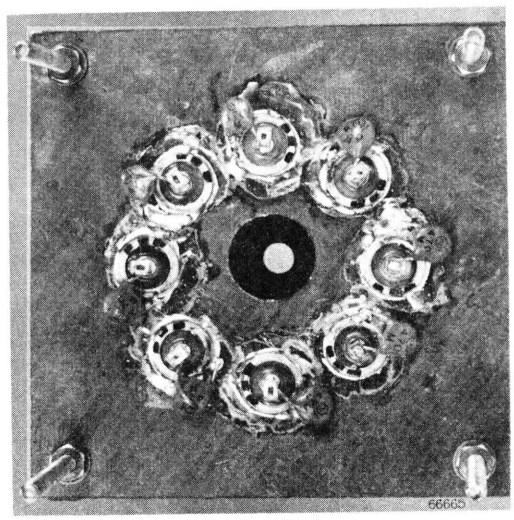
c. Three-pulse group; vertical scale 5 A/div., horizontal scale 5 nsec/div.

Fig. 11 - Output waveforms of the model A pulse generator

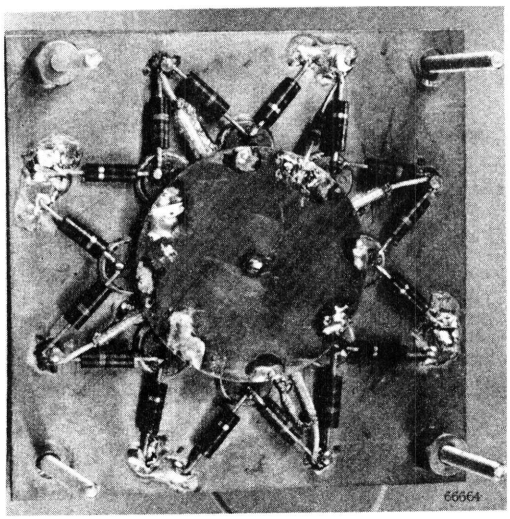
approximately 10 kpps. The charging circuitry consists of eight 650-pF ceramic capacitors. Electrical connection is again made by a pressure contact against the transistor headers. Lead lengths are kept as short as possible, although a large connection plate (Fig. 12c) is used to provide the low-inductance connection between paralleled transistors and the load. Avalanche synchronization is controlled by eight voltage dividers, and toggle switches are inserted at the bias terminals as a means of turning on or off individual transistors. Thus, the model B pulse generator can provide a variable-amplitude, single-pulse waveform by synchronously avalanching from one to eight transistors (Fig. 13a). Relatively continuous control of pulse-current amplitude may be made from 5 to 35 amperes by adjusting bias levels and combining avalanche stages. Maximum output (Fig. 13b) is a 44-ampere, 8-nsec-rise-time, 20-nsec-duration current pulse into a laser diode in series with a one-ohm sampling resistor. The peak-pulse current was less than



a. Complete pulse-generator assembly

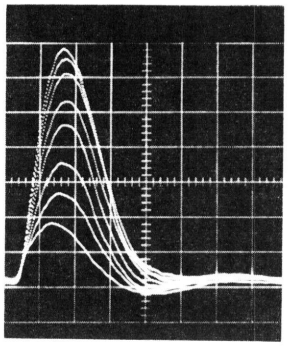


b. Charging capacitors

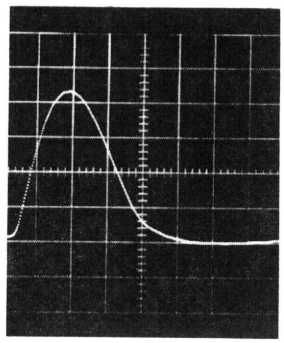


c. Connection plate

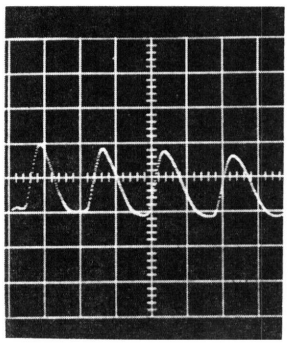
Fig. 12 - Construction of the model B pulse generator



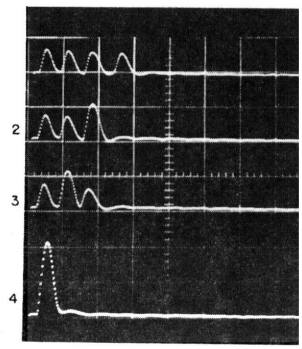
a. Single pulses, a total of one through eight transistors sequentially brought into avalanche; vertical scale 5 A/div., horizontal scale 10 nsec/div.



b. Single maximum current pulse, r.t. 8 nsec, duration 20 nsec, amplitude 44 A; vertical scale 10 A/div., horizontal scale 10 nsec/div.

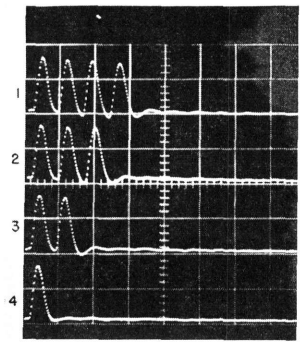


c. Four-pulse group with equal spacing; vertical scale 5 A/div., horizontal scale 10 nsec/div.



d. Illustration of pulse-delay variations which may be produced by adjusting collector bias levels; vertical scale 10 A/div., horizontal scale 5 nsec/div.
1. Four-pulse group, equal spacing
2. Fourth pulse coincident with third pulse
3. Fourth pulse coincident with second pulse
4. Synchronous avalanche, four pulses coincident

Fig. 13 - Output waveforms of the model B pulse generator (Cont.)



e. Pulse groups produced by turning off collector biases of individual transistors; vertical scale 5 A/div., horizontal scale 50 nsec/div.

f. Illustration of a technique for canceling negative transients; vertical scale 5 A/div., horizontal scale 20 nsec/div.
1. Main pulse followed by a negative transient
2. Negative transient cancelled by a delayed positive pulse

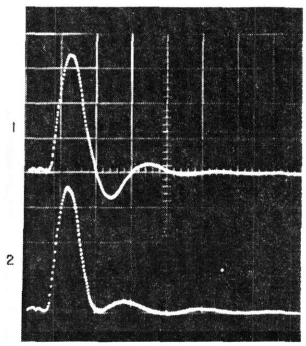


Fig. 13 - Output waveforms of the model B pulse generator

expected from the eight paralleled transistors, and the individual stage pulse rise times were degraded. These results are attributed to two factors: the presence of excess series inductance in the discharge circuit, and the tendency of the avalanche transistors to fire slowly and with decreased amplitude due to the dynamic retarding bias produced across the emitter-to-ground load circuit.

Figure 13c shows a four-pulse group which may be produced by the generator when it is triggered by a 200-nsec-rise-time pulse. The avalanche delays between the pulses can be varied (Fig. 13d) by adjusting the collector bias levels, and individual pulses may be turned off (Fig. 13e) by removing collector voltage from the corresponding transistor. Finally, Fig. 13f illustrates the technique of cancelling a negative transient which was previously described in Fig. 8.

CONCLUSIONS

A compact, high-current, nanosecond pulse generator for driving low-impedance devices can be made using standard transistors and components. By means of a simple collector biasing technique, suitable transistors (e.g., type 2N3020) can be paralleled and synchronized to switch simultaneously in the avalanche mode. Pulse currents with rise times comparable to avalanche transistor switching speeds may be produced if good high-frequency pulse techniques are applied. In the two pulse generators developed, control over output pulse waveshape and amplitude is accomplished by varying the number of paralleled transistors and adjusting collector biases. The biasing technique can also be applied to cancelling negative-going transients, and to generating pulse groups with variable pulse-to-pulse spacing. This type of pulse generator might be used as the driving source for the injection laser transmitter of a PCM or PPM optical communication system.

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REFERENCES

1. Austin, M.E., et al., "GaAs Laser Radar Components and Techniques," Lincoln Lab. Tech. Report 407, Oct. 29, 1965

2. Everest, F.G., "The Generation of High Current Pulses of Short Duration for Use with GaAs Lamps and Lasers," IEE Conference Pub., p. 51, 1964

3. Broom, R.F., "A Compact Pulse Generator for Driving Gallium Arsenide Lasers at Room Temperature," J. Scientific Instruments 42:123 (1965)

4. Ivekovic, D., "A Triple Subnanosecond Pulse Generator with Avalanche Transistors and Charge-Storage Diodes," Nuclear Instruments and Methods 32:339-340 (1965)

5. Prince, P.R., "Paralleling Avalanche Transistors," Proc. IEEE 53:304 (Mar. 1965)

6. Haas, I., "Millimicrosecond Avalanche Switching Circuits Utilizing Double-Diffused Silicon Mesa Transistors," Fairchild App. Data, App.-8

7. Karlsons, D., Reno, C.W., and Hannan, W.J., "Room-Temperature GaAs Laser Voice-Communication System," Proc. IEEE 52:1354-1355 (Nov. 1964)

8. Dill, H.G., "Avalanche Pulse Generators," Semiconductor Products, Feb. 1962

   a. p. 27
   b. pp. 23-30

9. Haas, I., "2-ns. Rise Time Pulses Obtainable from Fairchild 2N696-2N697 Si Mesa Transistors in Avalanche Mode," Fairchild App. Data, App.-1

10. Millman, J., and Taub, H., "Pulse, Digital, and Switching Waveforms," New York: McGraw-Hill, p. 202, 1965

11. Shaver, F.H., "A Fast-Rise, High-Current Transistor Pulse Generator," Semiconductor Products, pp. 29-34, Oct. 1962

12. "Avalanche Circuits are More Versatile than you Think," National Semiconductor Company, Engineering Memo. 15, June 8, 1964

13. Bell, B.H., "Avalanche Transistor Switching Circuits," National Semiconductor Company, Engineering Memo. 12, March 1963

14. Skilling, H.H., "Electrical Engineering Circuits," New York:Wiley and Sons, p. 473, 1957

GLOSSARY OF TERMS

BV_{CBO}	Collector-to-base diode breakdown voltage with emitter open
BV_{CER}	Collector-to-emitter diode breakdown voltage with base return resistance
BV_{CEO}	Collector-to-emitter diode breakdown voltage with base open
C_1	Charging capacitance
I_B	Base current
I_C	Collector current
I_L	Load current
I_P	Peak pulse current
LV_{CER}	Avalanche latching voltage
L_C	Critical series inductance
R_B	Base return resistance
R_L	Load resistance
R_{LT}	Total series load resistance
r_{ce}	Dynamic avalanche collector spreading resistance
R_1	Collector bias resistance
t_r	Pulse risetime
t_d	Pulse duration
V_C	Collector voltage
V_{CC}	Collector bias voltage
V_{CE}	Collector-to-emitter voltage
V_P	Peak pulse voltage

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13. ABSTRACT

A nanosecond, high-current pulse generator using paralleled avalanche transistors has been designed, and its operating characteristics have been determined. The generator utilizes the regenerative switching action of avalanching transistors to discharge capacitors through a low-impedance load. Transistors are selected for high collector-to-base diode breakdown voltage, BV_{CBO}, low avalanche latching voltage, LV_{CER} and fast avalanche switching. Control of the switching times of individual avalanche transistors is achieved by adjusting collector bias levels. This technique allows a variety of pulse waveforms to be generated, including pulse groups with adjustable pulse-to-pulse spacings. Output pulse waveforms are characteristic of a slightly underdamped RLC series circuit.

Two models of the generator were developed using standard transistors and components. Peak pulse currents on the order of 40 amperes, with rise time less than 10 nsec and repetition rates greater than 10 kHz, were produced in loads of approximately one ohm. The generators are suitable for pulse modulating low-impedance devices such as GaAs room-temperature injection lasers.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Pulse generators						
Nanosecond pulses						
High-current pulses						
Avalanche transistors						
Paralleled transistors						
Switching circuits						
Synchronized switching times						