Cree SiC Power White Paper:

The Characterization of dV/dt Capabilities of Cree SiC Schottky diodes using an Avalanche Transistor Pulser

Introduction

Since the introduction of commercial silicon carbide (SiC) Schottky diodes over 10 years ago, significant improvements in power factor correction (PFC) circuits and motor drives have been realized due to the elimination of minority carrier reverse recovery charge and its resulting switching loss associated with traditional PiN diodes. The early adoption of SiC Schottky diodes was somewhat hampered due to reliability issues, caused by unforeseen dV/dt limitations of the device. In particular, devices with lower dV/dt capability are more susceptible to failure from large in-rush currents. An initial investigation into the dV/dt of 600V SiC Schottky diodes found the upper limit of dV/dt to be 55-60V/ns (Volts per nanosecond) for these devices. As the diodes used in that study were not Cree® SiC Schottky diodes, follow-up studies were performed by researchers at Cree on their own 600V SiC Schottky diodes [1,2]. Their analysis found that the Cree diodes could withstand a turn-on rate of 75V/ns and a turn-off rate of 100V/ns for more than 100,000 cycles without failure. The end result of these and other studies is a motivation by diode manufacturers to report dV/dt ruggedness as a measure of SiC Schottky diode reliability.

The purpose of this work is to design a high speed, high voltage pulse generator (pulser) and use this pulser to demonstrate the dV/dt ruggedness Cree's Silicon Carbide diodes. Since the Cree diodes did not fail during prior referenced testing, a faster pulser is required to drive the diodes to their limits. This pulser would be capable of stressing the test devices at a dV/dt significantly faster than what would be experienced in normal power conversion applications. The original experiments performed at Cree used switching times of approximately 5ns. Pulsers with switching times approaching 1ns can be achieved by employing currently available avalanche transistors and Cree C2M™ SiC MOSFETs. The design, construction and test of the high speed pulser will be described along with the measured dV/dt ruggedness of Cree 600V and 1200V SiC Schottky diodes.

Application Considerations

The dV/dt ruggedness is one of the design factors that set the limits on achievable switching speed in hard switched applications. This can be illustrated by considering a very popular application of SiC devices, a power factor correction circuit (PFC) as shown in figure one. The maximum switching speed of MOSFET M1 is limited by the maximum dV/dt of the boost diode, D1. In this example, the turn-on loss experienced by M1 will be considered for the case of two diodes, each with different dV/dt limits, 50V/ns and 100V/ns. This first order analysis assumes ideal components (no parasitics) and perfectly linear switching. The initial condition is that MOSFET M1 is off; 20A of current is flowing through L1 causing D1 to conduct and the current flows out to the load. The voltage across C2 is 800V. When M1 turns on, D1 is rapidly reverse biased and the dV/dt limit on D1 (50V/ns or 100V/ns) sets the maximum turn on drain to source (V_{DS}) dV/dt of the MOSFET.

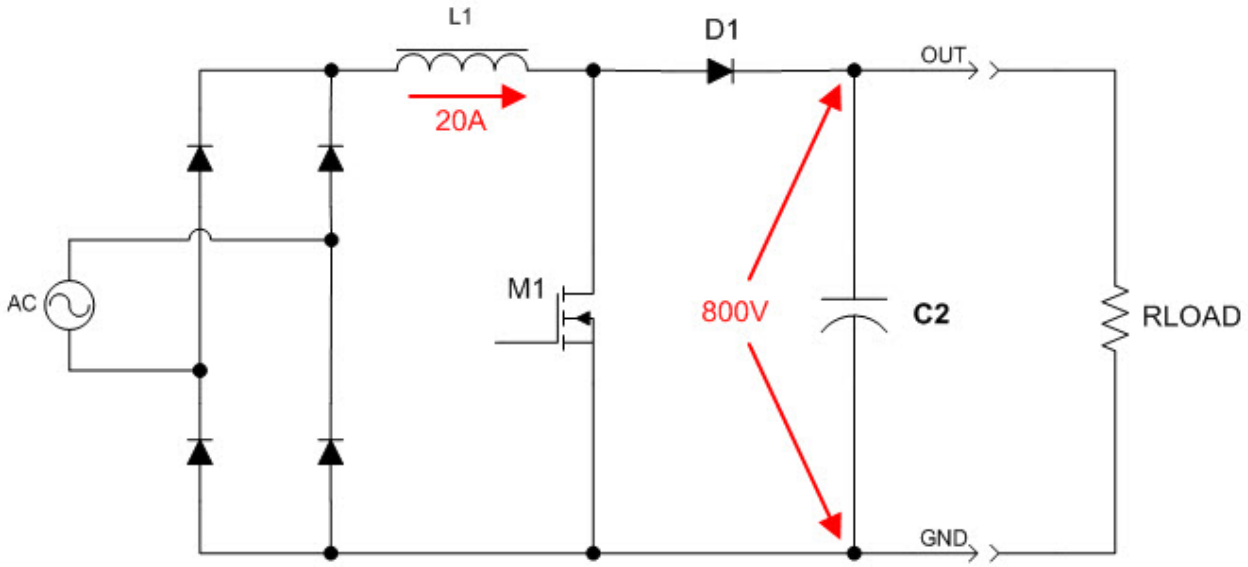

Figure 1: Basic PFC application

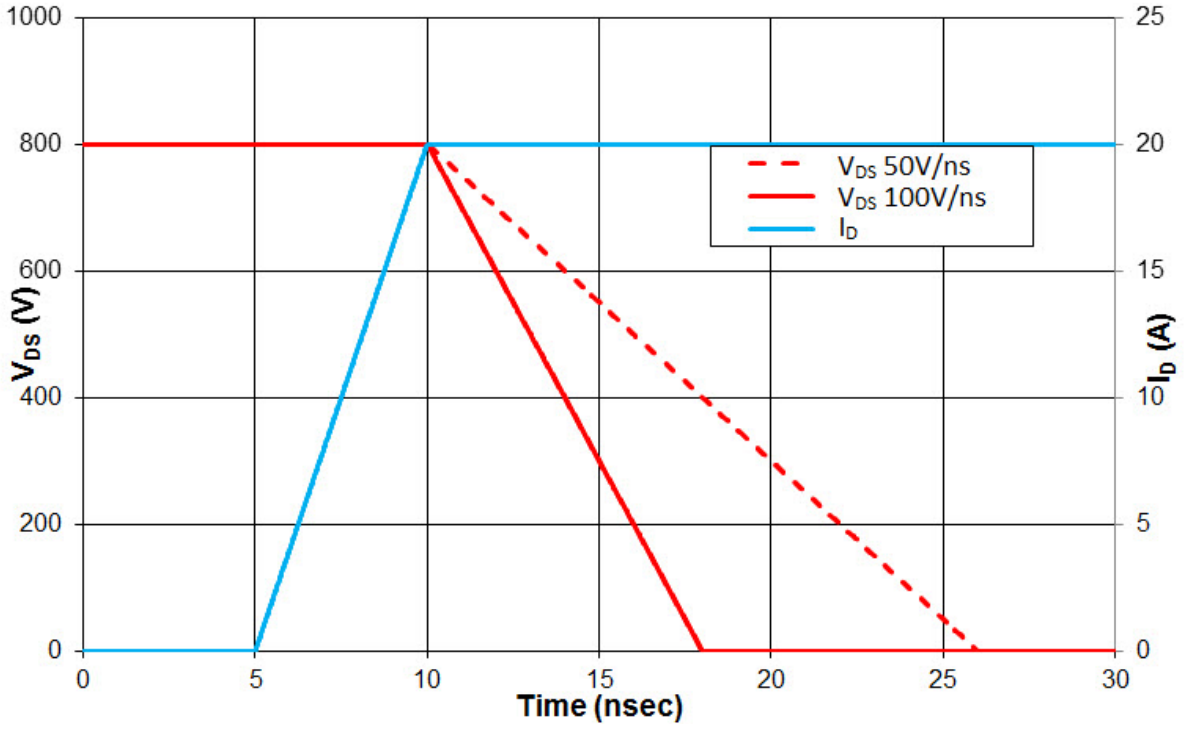

Figure 2: Ideal MOSFET turn-on waveforms for dV/dt limits of 50V/ns and 100V/ns

The turn-on V_{DS} and drain current (I_D) of the MOSFET is illustrated in figure two. The two cases for dV/dt are shown (the dV/dt is shown as a negative value because the voltage is falling). The current risetime is assumed to be the same for both cases. The MOSFET's instantaneous power ($P = I*V$) and switching energy ($E = \int P\,dt$) were calculated based on these waveforms and the results are shown in figure three.

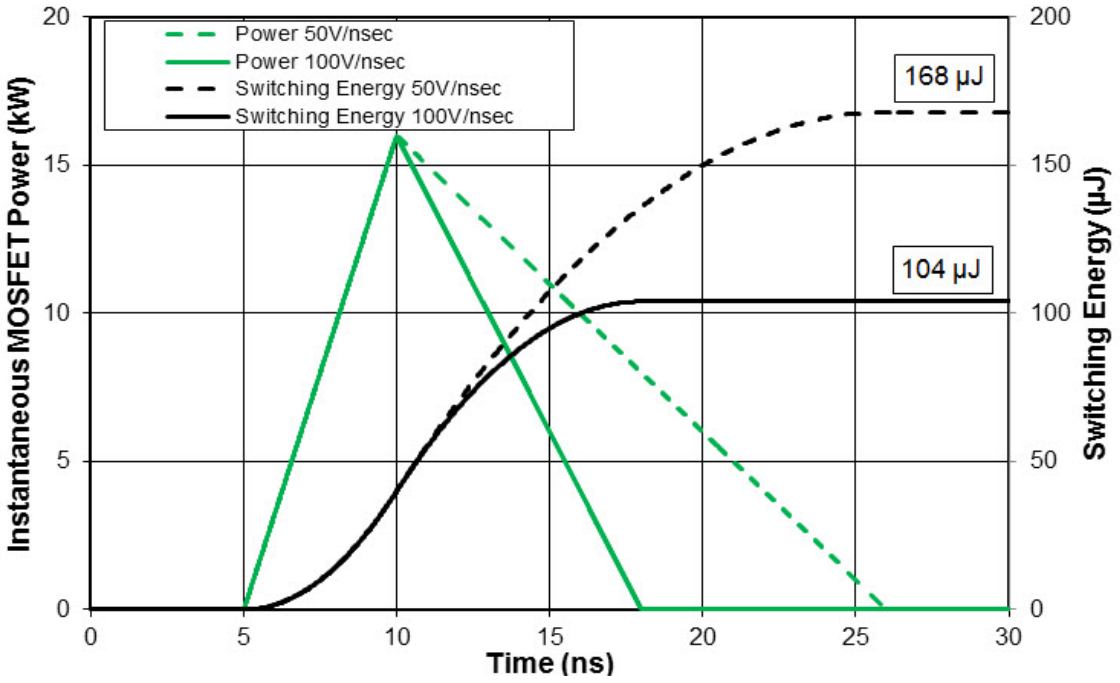

Figure 3: Instantaneous power dissipation and turn-on energy loss for 50V/ns and 100V/ns

The peak instantaneous power remains the same for the two cases. Additionally, the instantaneous power is the same during the current rise of the switching event (t = 5 ns to 10 ns). However, the time it takes the power to drop to zero is twice as long for the 50V/ns case. The switching energy during the current rise time (5 to 10 ns) is the same for both cases. The major difference in switching energy occurs during the voltage fall time (time > 10 ns). The switching energy for the 50V/ns case during this time period is twice as high, as compared to the 100V/ns case. Of course, this difference has a strong influence on the total switching energy. The total switching energy for the 50V/ns case is 168 µJ compared to 104 µJ for the 100V/ns – a 61.5% increase. Note that system switching losses are equal to the switching frequency multiplied by the switching energy. Therefore, the significant difference in switching energy for the two cases illustrates the need for higher dV/dt ruggedness to minimize switching losses, maximize system efficiency, and possibly even enable higher switching frequencies.

Series-Connected Avalanche Transistor Pulser for dV/dt Ruggedness Tests

The evaluation of dV/dt ruggedness requires a means of generating a very fast high voltage pulse. Some techniques include mercury wetted relay pulse generator [3] and avalanche transistors [4-12]. The mercury wetted relay approach has been historically used to generate extremely fast pulses. Unfortunately, a custom relay design would be required to handle the high voltages necessary in this study. A second widely used approach involves operating bipolar junction transistors (BJT) in avalanche breakdown region. This occurs when the BJT's collector to emitter voltage (V_{CEO}) is exceeded and the transistor enters secondary breakdown. By limiting the time the BJT is subjected to secondary breakdown, the device can be used as a very fast low-jitter high-voltage switch. This approach could be used to characterize the dV/dt ruggedness of SiC power devices, but the performance and reliability of common BJTs is not guaranteed for repeated operation in this mode. Alternatively, avalanche transistors are BJTs designed specifically for avalanche mode operation. Avalanche transistor pulsers are widely used to drive Pockels cells, streak cameras, lasers, etc., and are an excellent choice for this study. A popular configuration for high voltage avalanche transistor pulsers is the seriesconnection generator.

A series-connected avalanche transistor pulser was evaluated for the purpose of this work. The pulser was evaluated using a 200 Ω resistive load, and the circuit schematic is shown in figure four. Voltage measurements were taken with a high voltage probe connected directly to the BNC connector with an adapter to eliminate the ground wire inductance. Waveforms were observed with a 350MHz (1ns rise time) digital sampling oscilloscope with 400MHz 100:1 probe (900 psec rise time). The frequency response limitations of the oscilloscope and probe resulted in a system rise time of 1.35 ns.

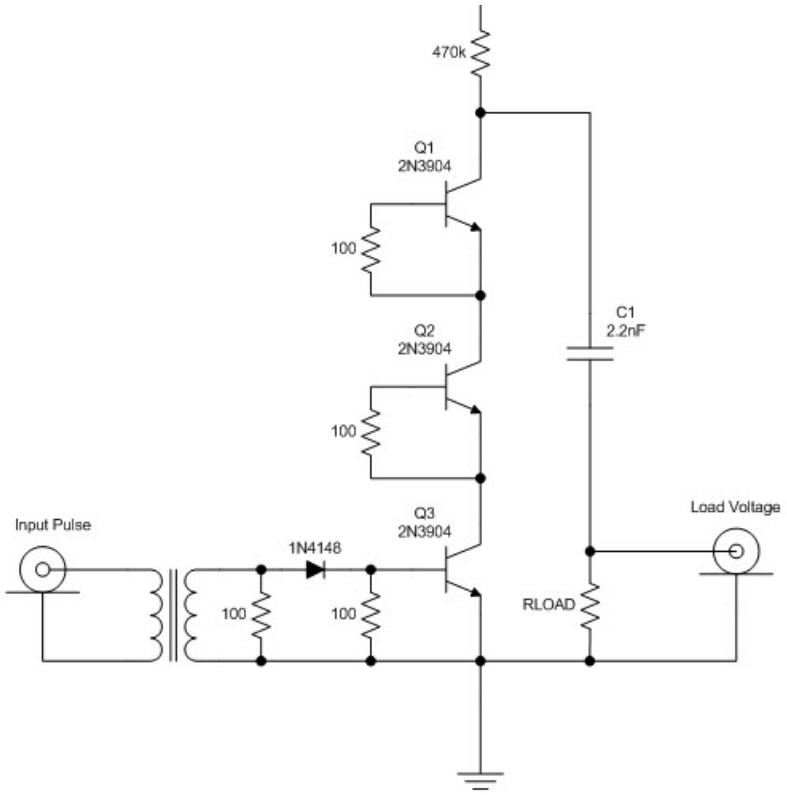

Figure 4: Pulse generator using series connected avalanche transistors

The circuit places three transistors with a maximum V_{CEO} of 40V in series. At steady state, the 400VDC input voltage is divided equally among the transistors resulting in a collector to emitter voltage (V_{CE}) of 133V across each transistor, placing them very close to avalanche. Operation of the circuit is as follows: a pulse is applied to the input and causes transistor Q3 to avalanche. Similar to a "domino effect", this action essentially causes the two remaining transistors to avalanche. This causes the top terminal of capacitor C1 to discharge to ground in less than 2ns. The result is that a high dV/dt negative-going pulse is produced across the load resistor (RLOAD). The output voltage pulse is presented in figure five, where the 1.35ns rise time is observed.

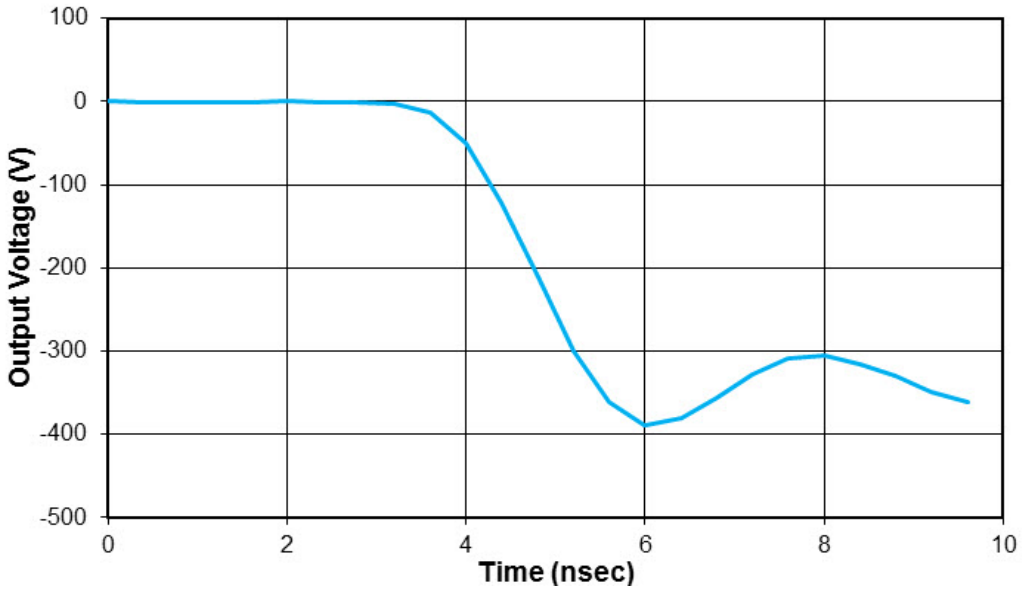

Figure 5: Series connected pulse generator output terminated into 200Ω RLOAD

SiC Schottky Diode dV/dt Ruggedness Testing

With a verified high-speed pulser in place, a series of dV/dt ruggedness tests were conducted on a Cree C3D03060A 600V 3A Schottky diode. The intent of the tests was to use the new setup to exercise the C3D03060A with a very fast pulse to see what the eventual dV/dt limitation was. This would give improved indication of the dV/dt ruggedness of the C3D diode line, compared to prior work. The series-string avalanche pulser was equipped with 2N5551 silicon bipolar transistors (max VCEO=160V) in order to achieve higher transition voltages, and the 200Ω resistor (RLOAD) was replaced with the diode, or DUT (device under test). The test pulse for the diode was set to 800V. A schematic of the test setup is shown in figure six, and the results of the test are shown in figure seven.

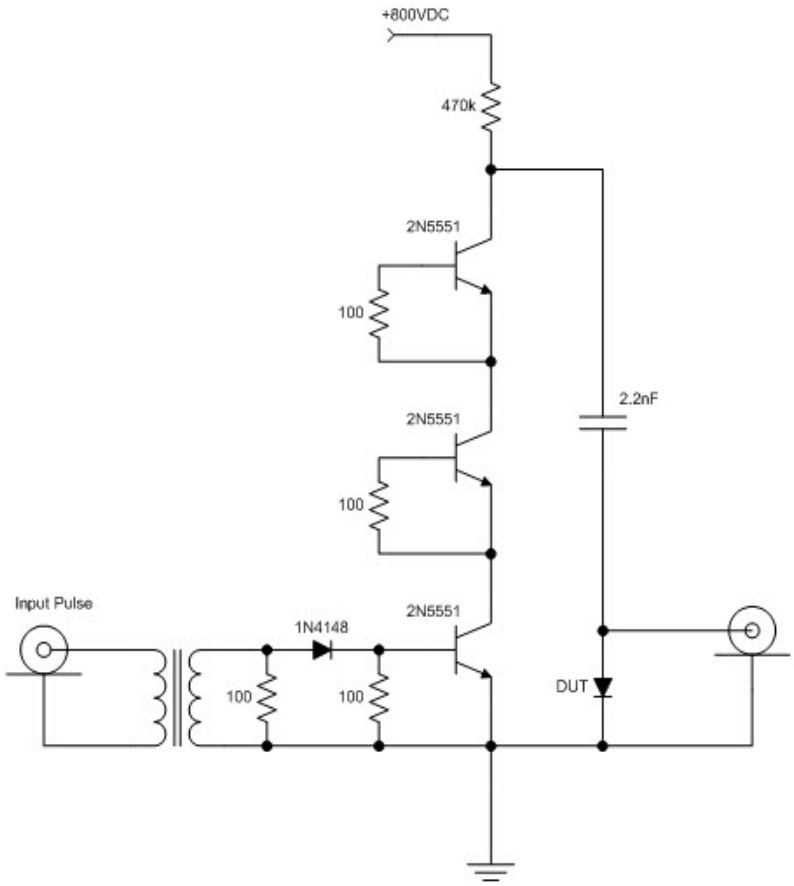

Figure 6: Schematic for the C3D03060A dV/dt ruggedness test setup

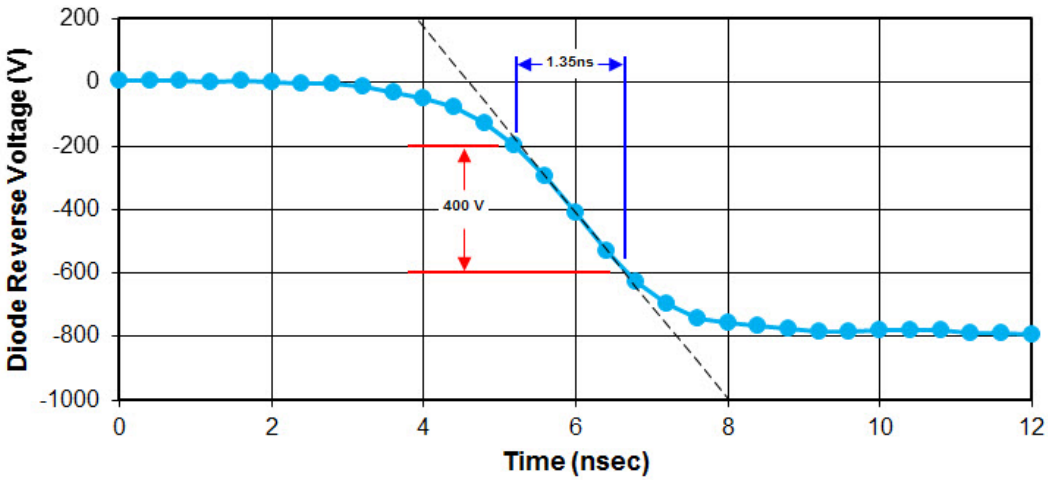

Figure 7: C3D03060A reverse dV/dt = 295 V/ns

The measured reverse (turn-off) dV/dt was 295 V/ns. This is about six times faster than the typically reported 600V diode dV/dt ruggedness specification of 50V/ns [13]; it is also roughly three times greater than the previous measurements taken by Cree. As before, no device failures were encountered during the course of these tests. These results clearly demonstrate the dV/dt ruggedness of the C3D03060A diode and give a clear indication of the ruggedness of the general C3D family. Further testing of additional devices is required for confirmation, but based on these results, the dV/dt ruggedness Cree's C3D Schottky diode family exceeds 300V/ns.

The logical next step was to perform the same testing on Cree's 1200V C4D family of diodes, in order to gain an indication of the dV/dt ruggedness of the C4D diode line. The DUT for these tests was a Cree C4D10120A 1200V 10A diode. The schematic of the test setup is shown in figure eight. The applied voltage (V_{DD}) was set to 1000V. Note that the pulse generator circuit had to be modified to account for V_{DD} and the rated V_{RRM} of 1200V of the C4D10120A, twice as large as that of the C3D03060A. Two of the 2N5551 silicon transistors have been replaced by a single Cree C2M0080120D SiC MOSFET. The SiC MOSFET is turned on quickly via a pulse applied to the remaining 2N5551 avalanche transistor. The activation of the SiC MOSFET causes the top terminal of the SMD capacitor to discharge to ground, resulting in a reverse bias pulse of 1000V to be applied to the DUT. The voltage was measured with the low impedance resistive divider to minimize ringing.

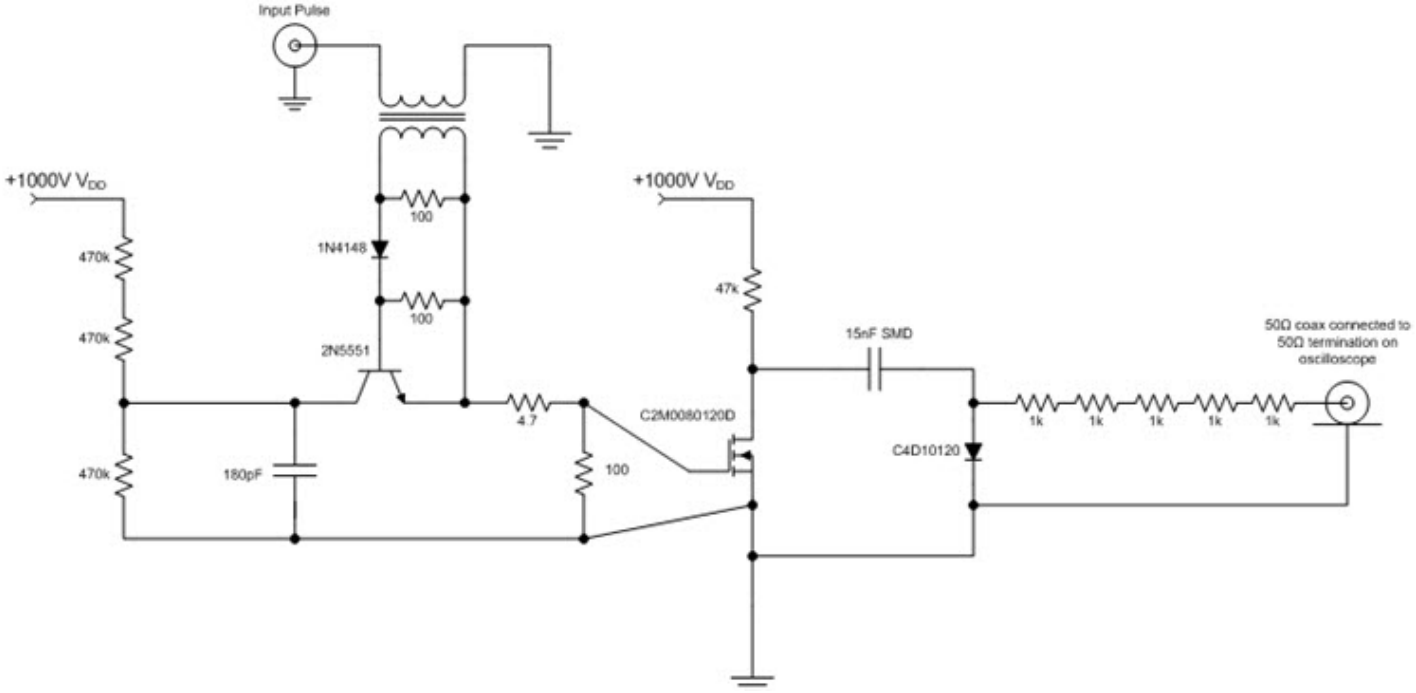

Figure 8: Schematic for the C4D10120A dV/dt ruggedness test setup

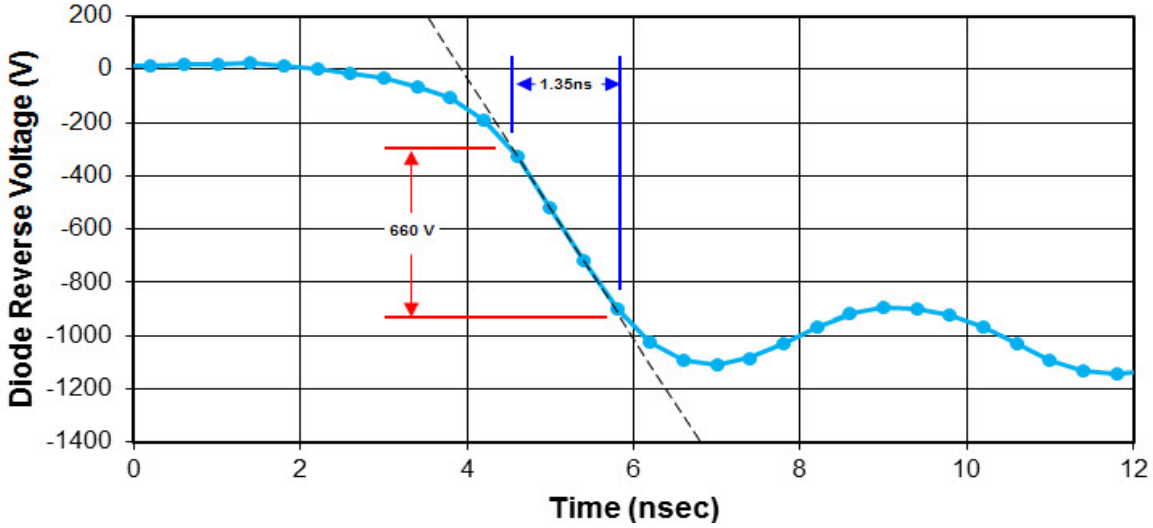

Figure 9: C4D10120A reverse dV/dt = 490 V/ns

As shown in figure nine, the measured reverse dV/dt was 490 V/ns. This is about six times faster than the typically reported diode dV/dt ruggedness value of 80V/ns of 1.2kV SiC JBS diodes [15]. No device failures were encountered during the course of these tests. These results clearly demonstrate the dV/dt ruggedness of the C4D10160A JBS diode and give a clear indication of the ruggedness of the general C4D family.

Conclusions

The dV/dt ruggedness of SiC Schottky diodes is a concern for many designers. The goal of this work was to design a faster pulser capable of subjecting the test devices to a dV/dt significantly faster than what would be experienced in practice, in order to further characterize Cree's C3D and C4D families of SiC Schottky diodes. Furthermore, the Cree diodes demonstrated six times higher dV/dt ruggedness than what is typically reported in the industry, with values of 295V/ns and 490V/ns, respectively. Most importantly, no failures were observed with any of the devices tested, which means the actual limits of the Cree diodes exceeds these values. As of this writing, the ultimate dV/dt ruggedness of these devices remains unknown.

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